HI5828EVAL2 User's Manual

Application Note | February 2000 | AN9855.1

Description

The HI5828EVAL2 evaluation board provides a quick and easy method for evaluating the HI5828, 125MSPS Dual High Speed DAC. Each converter outputs a current into a load resistor to form a voltage which can be measured by using the included SMA connectors. The amount of current out of the DACs is determined by an external resistor and either an internal or external reference voltage. The evaluation board also includes a VME (Versa Module Eurocard) digital interface that is compatible with all previous INTERSIL DAC evaluation boards. Transformers are included to take advantage of differential signal drive.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	CLOCK SPEED
HI5828EVAL2	25	Evaluation Platform	125MHz

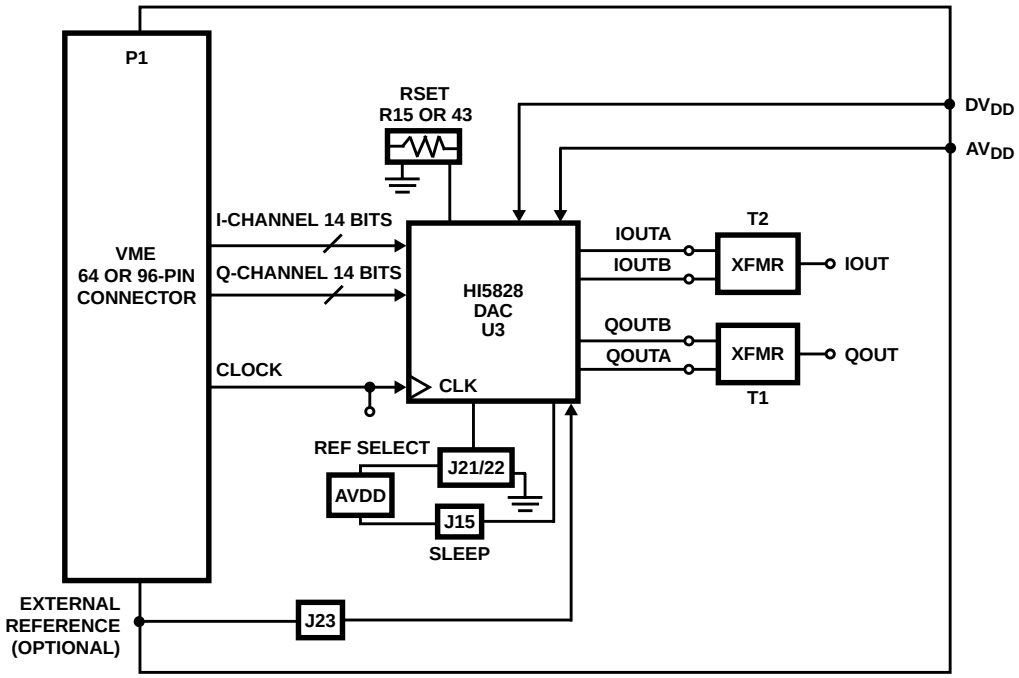
Features

- HI5828, Dual 12-Bit, 125MSPS CMOS DACs
- Single or Dual 3-5V Supply Range
- Future Dual 14-Bit Ready
- Standard VME/DSP Interface, HSP-EVAL Compatible
- SMA Outputs with Transformer Option
- Easily Selectable Internal or External Reference

Applications

- I and Q Signal Generation
- Modulated Carrier Generation
- General DAC Performance Evaluation
- Amplitude Modulation Via External Reference

Functional Block Diagram



Functional Descriptions

Voltage Reference

The HI5828 has an internal nominal 1.2V voltage reference with a ±10ppm/^{o}C drift coefficient over the industrial temperature range. The REFLO pin (18) selects the reference. Access to pin 18 is provided through solder jumpers J21 and J22. These jumpers are labeled INT and EXT for internal or external reference. The REFIO pin (17) provides access to the internal voltage reference and can be overdriven if the user wishes to use an external source for the reference. The internal reference was not designed to drive an external load. Notice that a 0.1µF capacitor is placed as close as possible to the REFIO pin. This capacitor is necessary for ensuring a noise free reference voltage.

If the user wishes to use an external reference voltage, jumper J23 must be in place and an external voltage reference provided via J18, an SMA connector labeled 'EXT REF'. Jumper J22 must be soldered so that pin 18 (REFLO) is tied to a logic high (the supply voltage). The recommended limits of the external reference are between 15mV and 1.2V. Performance of the converter can be expected to decline as the reference voltage is reduced due to the reduction in LSB current size.

If the user wishes to amplitude modulate the DAC, the REFIO pin can be overdriven with a waveform. The input multiplying bandwidth of the REFIO input is approximately 1.4MHz when driving a 100mV signal into the REFIO pin, biased at 0.6V_{DC}. The 3dB BW reduces as this amplitude is increased. It is necessary that the multiplying signal be DC offset so that the minimum and maximum peaks are positive and below 1.2V. The output current of the converter, IOUTA and IOUTB, is a function of the voltage reference used and the value of R_{SET}, R43.

Output Current

The output current of the device is set by choosing R_{SET} and V_{FSADJ} such that the resultant of the following equation is less than 20mA:

$I_{OUT} = 32 \times V_{FSADJ}/R_{SET}$.

REFIO (Pin 17) and FSADJ (Pin 20) of the DAC are the inputs to an operational amplifier. The voltage at the FSADJ pin (V_{FSADJ}) will be approximately equal to the voltage at the REFIO pin, which will either be the value of the internal or external reference. For example, using the internal reference of (nominal) 1.2V and an R_{SET} value of 1.91kΩ results in an I_{OUT} of approximately 20mA (maximum allowed). Choose the output loading so that the Output Voltage Compliance Range is not violated (-0.3 to 1.25V).

The output can be configured to drive a load resistor, a transformer, an operational amplifier, or any other type of output configuration so long as the output voltage compliance range and the maximum output current are not violated.

Transformer Output

The evaluation board is configured with a transformer output configuration, shown in Figure 1. This configuration was chosen because it provides: even harmonic performance improvement due to the complimentary differential signaling; ~12.5Ω R_{EQ} loading to each output of the DAC; drive impedance of 50Ω for matching with a spectrum analyzer; and 2x voltage gain. The output of this configuration will be biased at zero volts and have an amplitude of ~500mV (V_{OUT}) when the DAC is configured to drive I_{OUTFS} of 20mA.

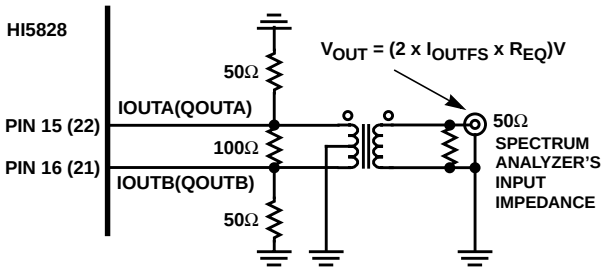


FIGURE 1.

Sleep

The converter can be put into 'sleep' mode by connecting pin 9 of the DAC to either of the converter's supply voltages. The sleep pin has an active pull-down current, so the pin can be left disconnected or be grounded for normal (awake) operation. On the evaluation board, jumper J15 is provided for controlling the sleep pin. Remove the solder jumper from J15 for normal operation and replace it for sleep mode.

Power Supply(s) and Ground(s)

The user can operate from either a single supply or from dual supplies. The supplies can be at different voltages. It is important to note that the digital inputs cannot switch more than 0.3V above the digital supply voltage. The evaluation board contains two power supply connections, (analog) AVDD and (digital) DVDD, each with their own ground wire. Dual ground and power planes is the recommended configuration, with the ground planes connected at a single point (J7 on the evaluation board). Error on the board: the labels for DGND and AGND are swapped. The DGND label is next to the analog ground connection and the AGND label is next to the digital ground connection.

Digital Inputs

The DAC is designed to accept CMOS inputs. The switching voltage is approximately 1/2 of the digital power supply voltage, so reducing the power supply can make the DAC compatible to smaller levels. The digital inputs (data and clock) cannot go +0.3V higher than the digital supply voltage, else diode ESD protection can begin to turn on and performance could be degraded. The clock source can be a sine wave, with some degradation in performance possible. The recommended clock is a square wave.

The timing between the clock and the data will effect spectral performance and functionality. Minimum setup and hold times are specified in the datasheet to represent the point at which the DAC begins to lose bits. Optimal setup and hold times vary with the clock rate to output frequency ratio. A general rule is that the lower the F_{CLK}/F_{OUT} ratio is, the higher the setup time should be to achieve optimum spectral behavior.

Getting Started

A summary of the external supplies, equipment, and signal sources needed to operate the board is given below:

1. +5V to +3V supply for HI5x60 DAC.
2. Pattern Generator.
3. Square wave clock source (usually part of the Pattern Generator).
4. Spectrum Analyzer or Oscilloscope for viewing the output of the converter.

Attach the evaluation board to the power supply(s). Connect the bits from the data generator to the evaluation board, preferably by using a male, 64 or 96-pin VME (Versa Module Eurocard) connector that mates with the evaluation board. Connect the clock source to the evaluation board, also preferably through the VME connector. Failure to make clean and short connections to the data input lines and clock source will result in a decrease in spectral performance.

Using a coaxial cable with the proper SMA connector, attach the output of the converter, I_{OUT}, to the measurement equipment that will be evaluating the converter's performance. Make sure that the jumpers are in their proper placement. Consult the 'Voltage Reference' section and the 'Sleep' section of this document for a definition of the jumpers' functionality.

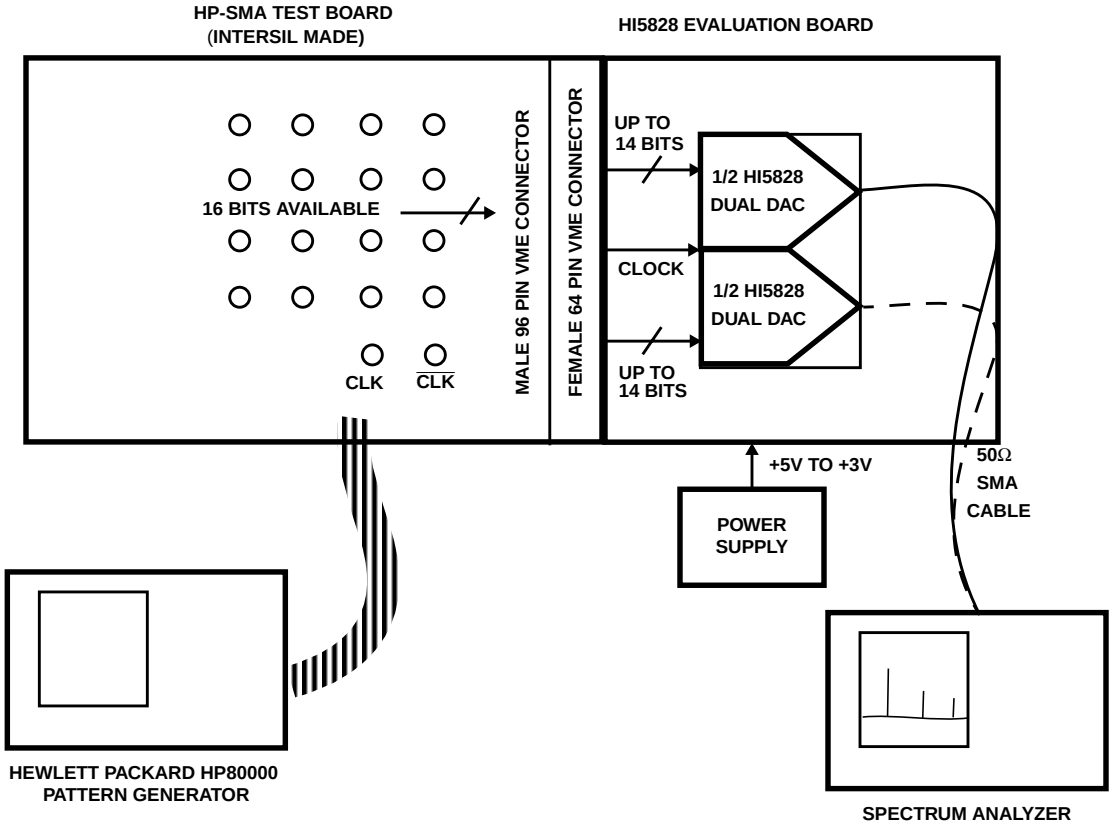


FIGURE 2. INTERSIL HI5828 EVALUATION SYSTEM SETUP BLOCK DIAGRAM

Appendix A Description of Architecture

The segmented current source architecture has the ability to improve the converter's performance by reducing the amount of current that is switching at any one time. In a segmented current source arrangement, transitions such as midscale become one in which you simply have an additional intermediate current source turning on and several minor ones turning off. In the case of the HI5760 10-Bit DAC, there are 31 intermediate current segments that represent the 5 MSBs and five, binary-weighted current sources representing each of the five LSBs. See the Functional Block Diagram in the datasheet for a visual representation. To relate the midscale transition example to the HI5760, consider the following: The code 0111111111 would be represented by 15 intermediate current segments and each of the 5 LSB current sources all turned on. To transition to code 1000000000 would simply require turning off the 5 LSB current sources and turning on the next intermediate current segment, bringing the total amount of current switching at this 'major' code transition equal to the same amount switching at 30 other code transition points in the code ramp from 0 to 1023, so that the total glitch energy is distributed more evenly. The HI5828 uses this technique but with a 5 MSB/7 LSB split.

HI5828 Pin Descriptions

PIN NO.	NAME	DESCRIPTION
11, 19, 26	AGND	Analog Ground.
13, 24	A_{VDD}	Analog Supply (+3V to +5V).
28	CLK	Clock Input. The master and slave latches shown in the functional block diagram are simple D-latches. Input data to the DAC passes through the "master" latches when the clock is low and is latched into the "master" latches when the clock is high. Data presented to the "slave" latch inputs passes through when the clock is high and is latched into the "slave" latches when the clock is low. This master-slave arrangement comprises an edge-triggered flip-flop, with the DAC being updated on the rising clock edge.
27	DGND	Connect to Digital Ground.
10	D_{VDD}	Digital Supply (+3V to +5V).
20	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}. Where V_{FSADJ} is the voltage at this pin. V_{FSADJ} tracks the voltage on the REFIO pin (refer to the functional block diagram); which is typically 1.2V if the internal reference is used.
14, 23	ICOMP1, QCOMP1	Compensation Pin for Use in Reducing Bandwidth/Noise. Each pin should be individually decoupled to AVDD with a 0.1µF capacitor. To minimize crosstalk, the part was designed so that these pins **must** be connected externally, ideally directly under the device packaging. The voltage on these pins is used to drive the gates of the PMOS devices that make up the current cells. Only the ICOMP1 pin is driven and therefore QCOMP1 needs to be connected to ICOMP1, but de-coupled separately to minimize crosstalk.
12, 25	ICOMP2, QCOMP2	Compensation Pin for Internal Bias Generation. Each pin should be individually decoupled to AGND with a 0.1µF capacitor. The voltage generated at these pins represents the voltage used to supply power to the switch drivers (refer to the functional block diagram) which is 2.0V nominal. This arrangement helps to minimize clock feedthrough to the current cell transistors for reduced glitch energy and improved spectral performance.
43-48, 1-6, 29-40	ID11-ID0, QD11-QD0	Digital Data Input Ports. Bit 11 is Most Significant Bit (MSB) and bit 0 is the Least Significant Bit (LSB).
15, 22	IOUTA, QOUTA	Current Outputs of the Device. Full scale output current is achieved when all input bits are set to binary 1.
16, 21	IOUTB, QOUTB	Complementary Current Outputs of the Device. Full scale output current is achieved on the complementary outputs when all input bits are set to binary 0.
7, 8, 41, 42	NC	No Connection.
17	REFIO	Reference voltage input if Internal reference is disabled. Use 0.1µF cap to ground when internal reference is enabled.
18	REFLO	Reference Low Select. To enable the internal reference, connect REFLO to analog ground. To disable the internal reference circuitry this pin should be connected to A_{VDD}.
9	SLEEP	Control Pin for Power-Down Mode. Sleep Mode is active high; connect to ground for Normal Mode. Sleep pin has internal 20µA (nominal) active pull-down current.

Appendix C Circuit Board Layout

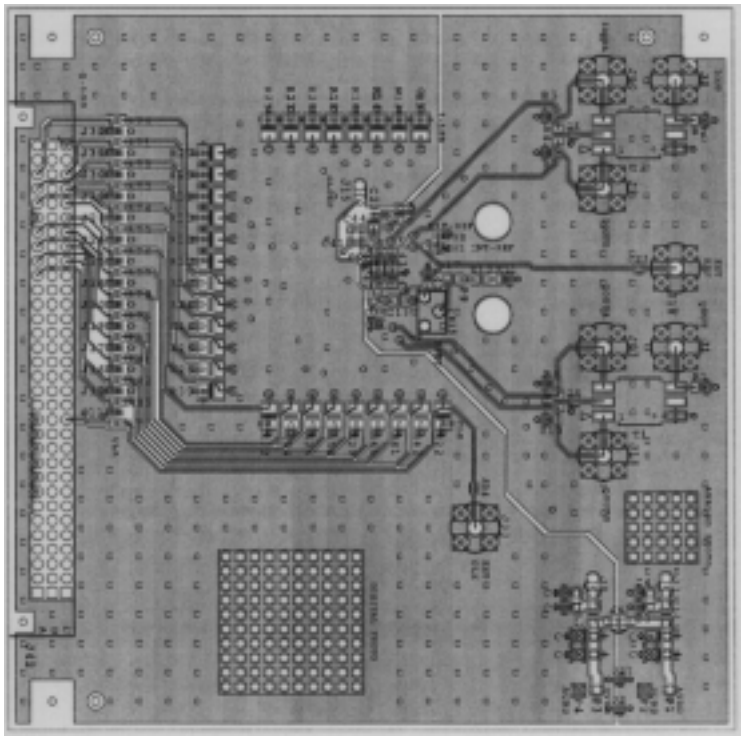


FIGURE 3. PRIMARY SIDE (VIEWED FROM THE TOP)

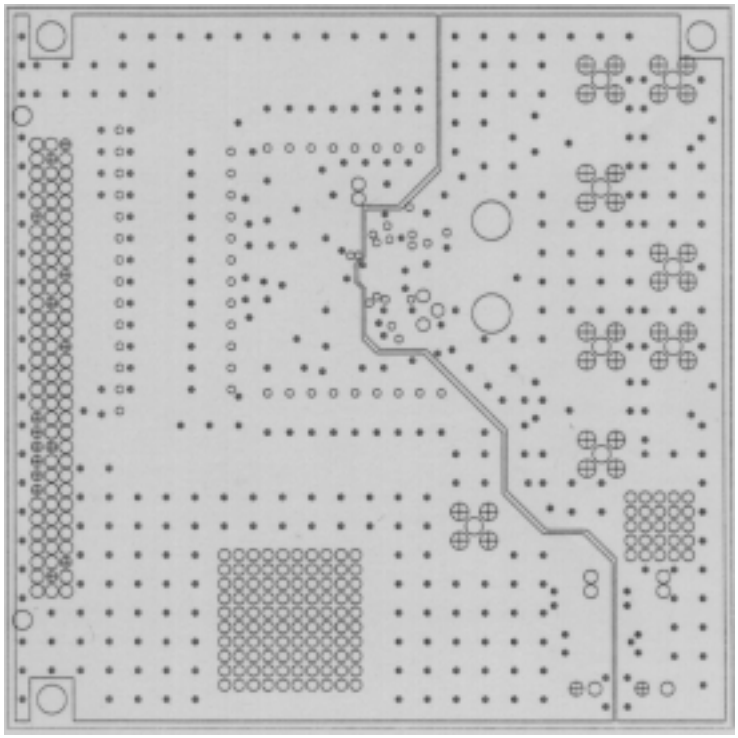


FIGURE 4. GROUND LAYER (2) (VIEWED THROUGH THE BOARD FROM THE TOP)

Appendix C Circuit Board Layout (Continued)

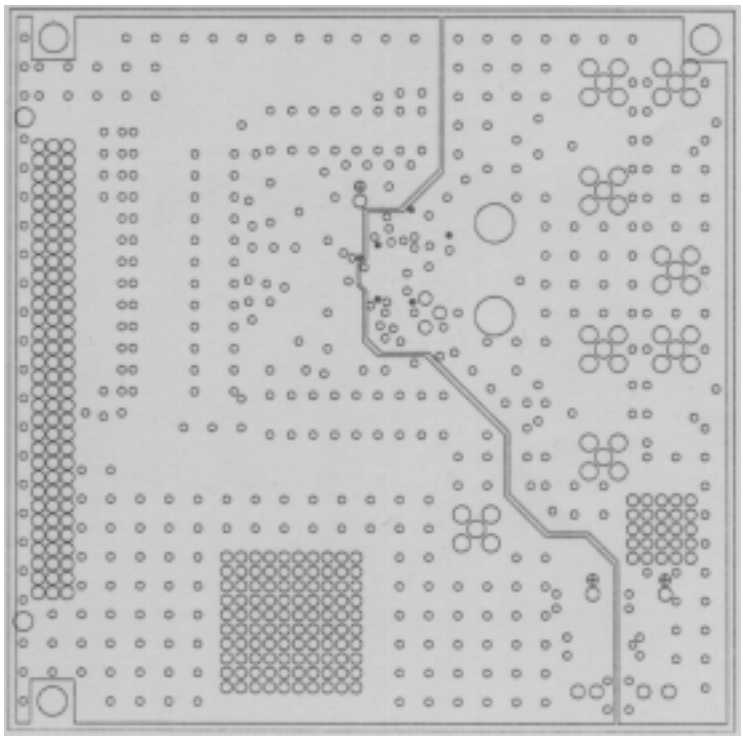


FIGURE 5. POWER LAYER (3) (VIEWED THROUGH THE BOARD FROM THE TOP)

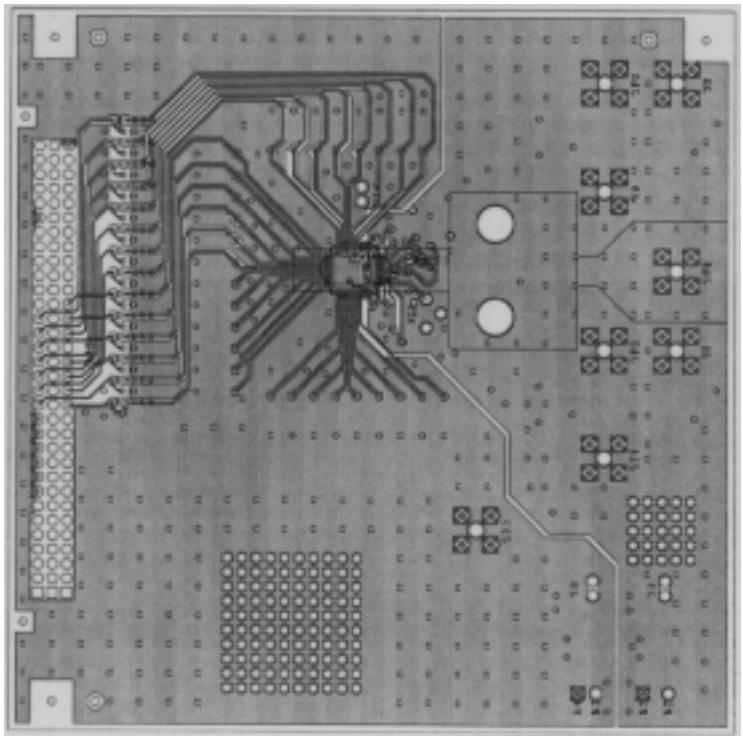
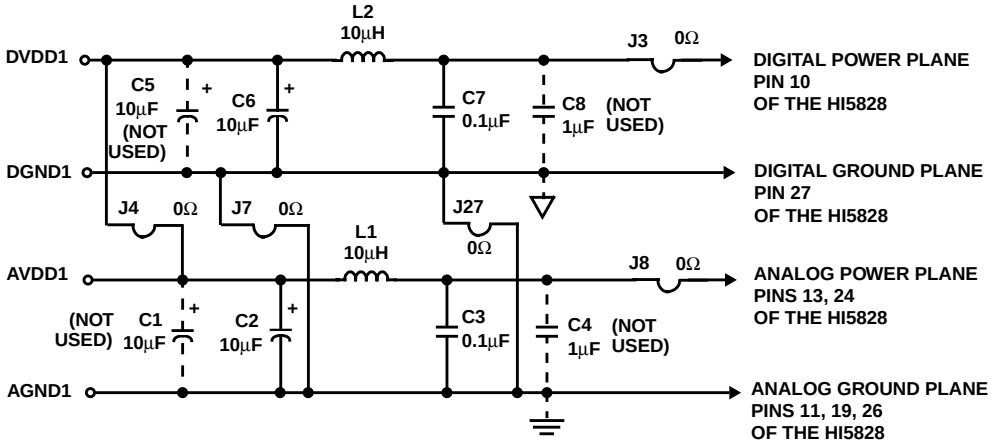


FIGURE 6. SECONDARY SIDE (VIEWED THROUGH THE BOARD FROM THE TOP)

Power Supply Input Circuit



NOTE: DV_{DD} and AV_{DD} can be tied together for single supply operation. AGND1 and DGND1 are tied together at a single point. See text for further explanation.

Ground Symbol Definition

= ANALOG GROUND (AGND1)

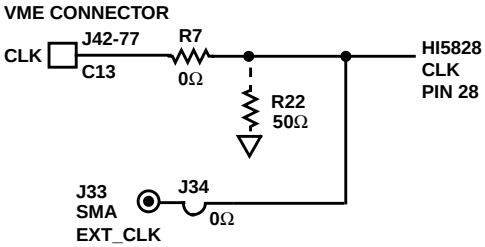
= DIGITAL GROUND (DGND1)

Digital Input Jumper Connections

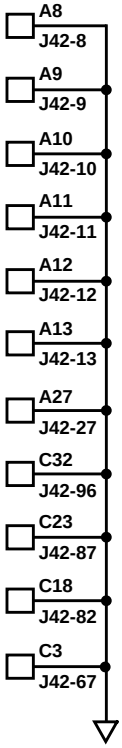
Q13	J11 0Ω I13	Q6	J25 0Ω I6
Q12	J12 0Ω I12	Q5	J26 0Ω I5
Q11	J16 0Ω I11	Q4	J28 0Ω I4
Q10	J17 0Ω I10	Q3	J29 0Ω I3
Q9	J19 0Ω I9	Q2	J30 0Ω I2
Q8	J20 0Ω I8	Q1	J31 0Ω I1
Q7	J24 0Ω I7	Q0	J32 0Ω I0

NOTE: These solder jumpers (J11, J12, J16....) are present so that the data channels can be connected together for driving both channels with one pattern generator.

Clock Input Circuit

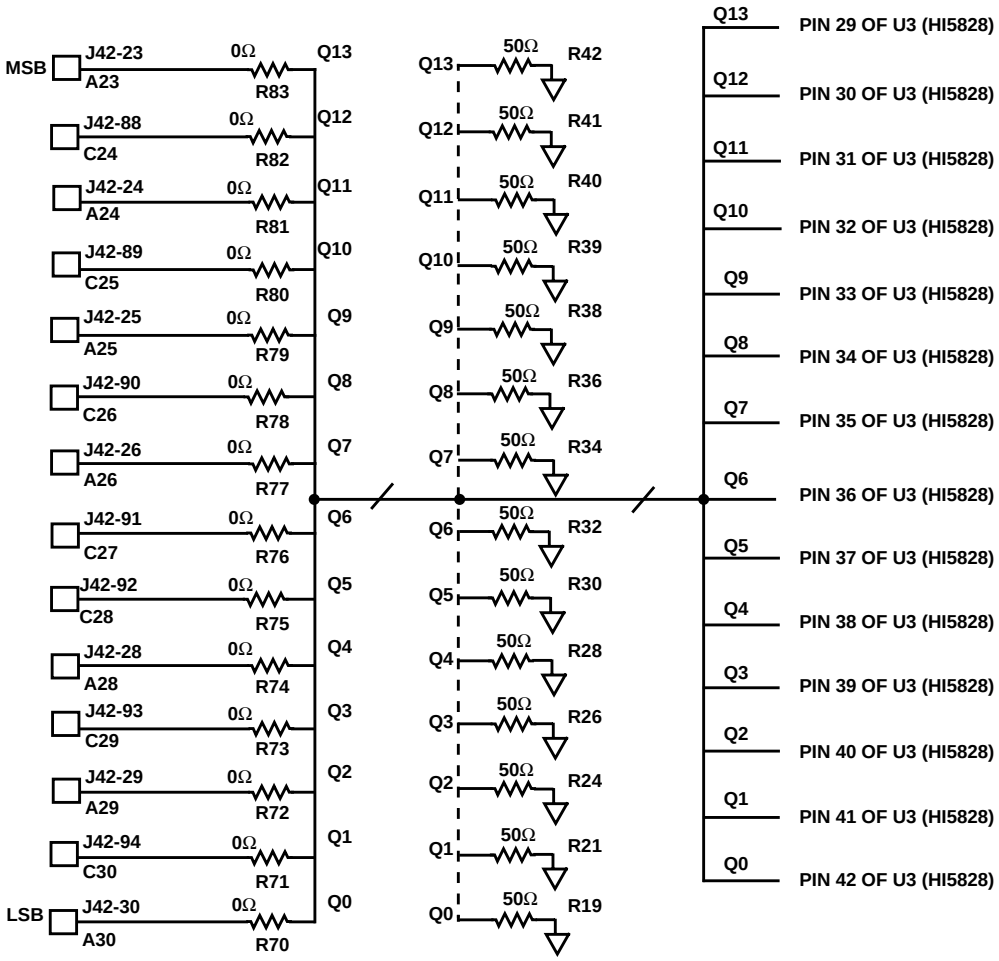


VME (Versa Module Eurocard) Ground Connections



Digital Input - Q Channel

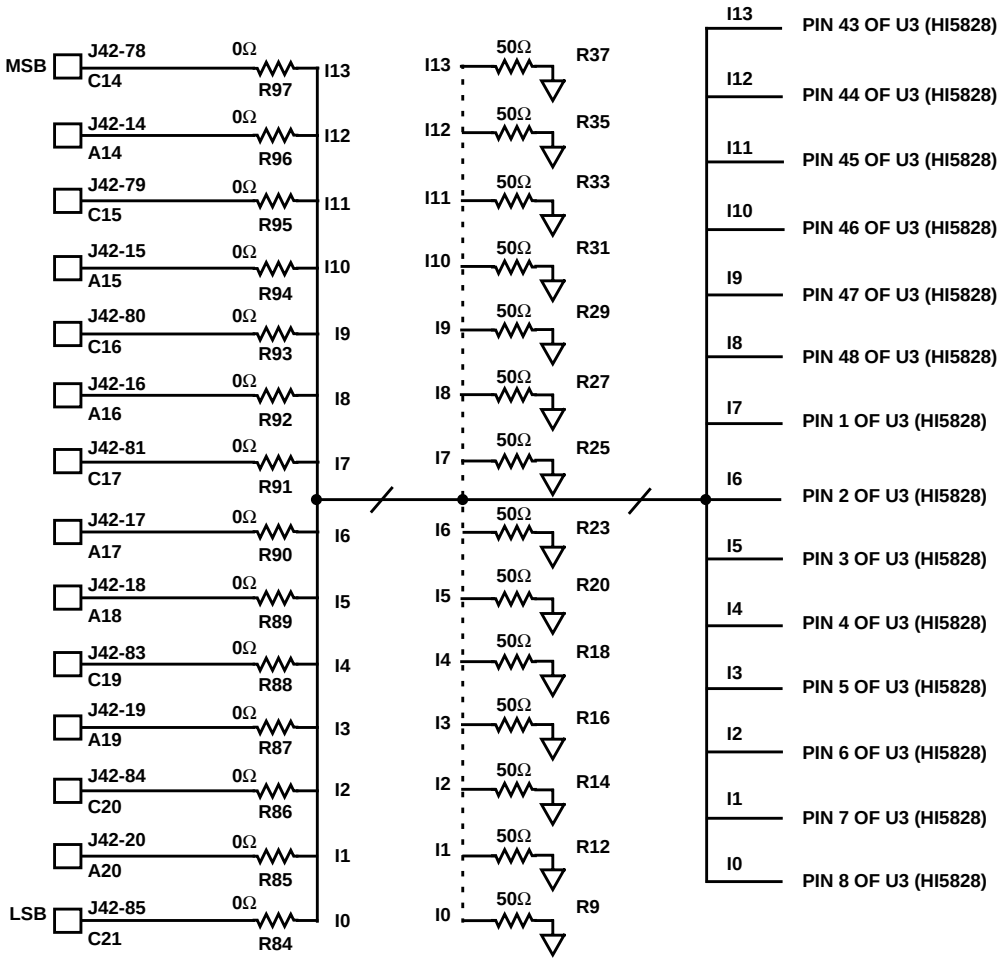
VME Connections



NOTE: The 50Ω terminations are recommended if the DAC'S performance is not as expected, especially for CLOCK > 50MSPS.

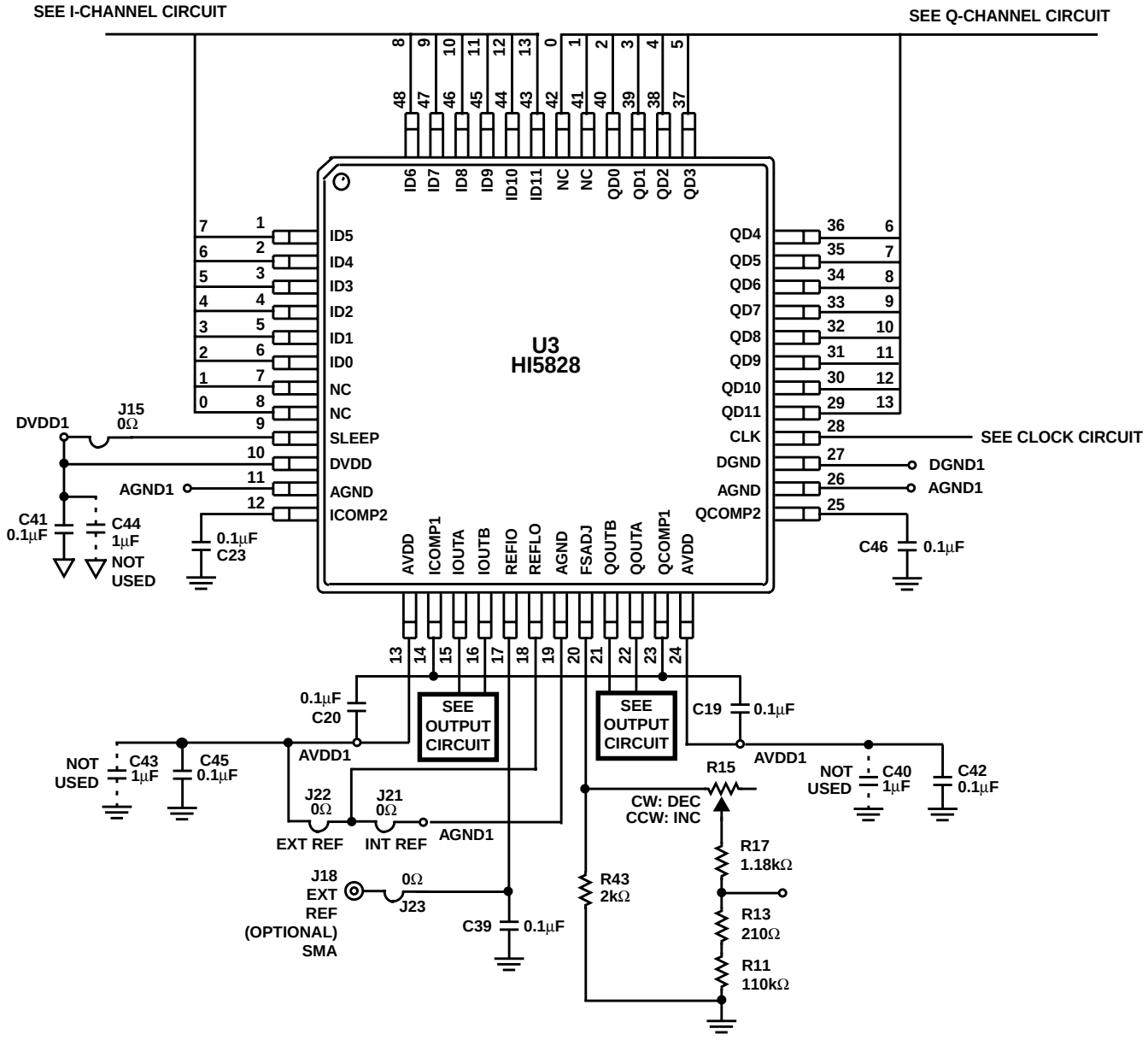
Digital Input - I Channel

VME Connections



NOTE: The 50Ω terminations are recommended if the DAC'S performance is not as expected, especially for CLOCK > 50MSPS.

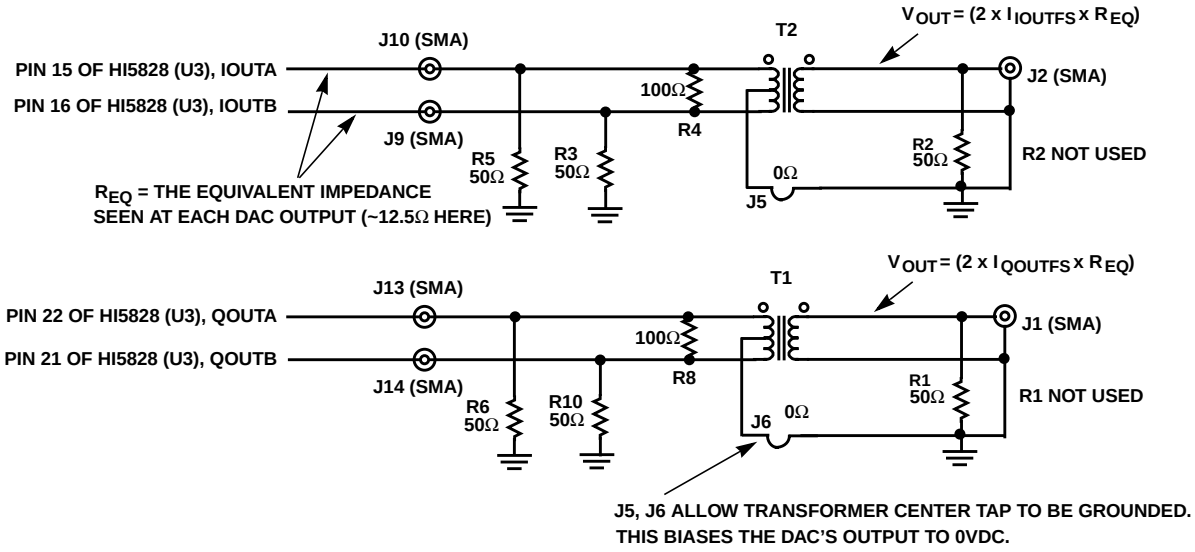
DAC Connections



NOTES:

1. ICOMP1 and QCOMP1 MUST be connected together externally. Also, the 0.1µF capacitors (C19 and C20) are recommended, but if the layout allows, a single capacitor placed directly between the ICOMP1 and QCOMP1 pins could serve both.
2. As with the COMP1 pins, a single 0.1µF capacitor could serve to decouple both of the AVDD pins (13 and 24) if placed directly between them. Else, it is recommended that each AVDD pin have its own capacitor to analog ground.

Differential-to-Single Ended Transformer Outputs, I and Q



Appendix D Evaluation Board Bill Of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION
U3	1	HI5828IN, Intersil Dual 12-bit D/A Converter, 48 Pin LQFP
C2, 6	2	10μF, Tantalum Chip Cap, SMD, 10%, 10V
C3, 7, 19, 20, 23, 39, 42, 44-46	10	0.1μF, Ceramic Chip Cap, 0805, 10%, 50V
C4, 8, 40, 41, 43 (Not Populated)	0	1μF, Ceramic Chip Cap, 0805, +80-20%, 16V
R9, 12, 14, 16, 18-42 (Not Populated)	0	50Ω, Chip Resistor, 1210, 5%, 1/4W
R7, 70-97 (R70, 71, 84, 85 Not Populated)	29	0Ω, Chip Resistor, 0805, 1/8W
R4, 8	2	100Ω, Chip Resistor, 0805, 1/8W
R3, 5, 6, 10 (R1, 2 Not Populated)	4	49.9Ω, Chip Resistor, 0805, 1/8W
R15 (Not Populated)	0	25kΩ, Potentiometer Res, 3296W, 1/4W, 10%
R43	1	1.91kΩ, Chip Resistor, 0805, 1/8W
J3, 8	2	1x2 Header
Header Jumper	2	1x2 Header Jumper
T1, 2	2	Mini-Circuits, T1-1T KK81, Z1:Z2 ratio of 1:1
J42	1	96-Pin Eurocard, Right Angle, Female
J1, 2, 9, 10, 13, 14 (J33 Not Populated)	6	SMA Straight Jack, PCB Mount
L1, L2	2	0Ω, Chip Resistor, 1206, 1/8W, 5%
J11, 12, 16, 17, 19, 20, 24-26, 28-32 (Not Populated)	14	Solder Jumpers (Connects I and Q input bits together for driving with the same pattern)
Mechanical Clamp (Not Populated)	0	DUT Clamp
Plastic Standoffs	4	3/4"