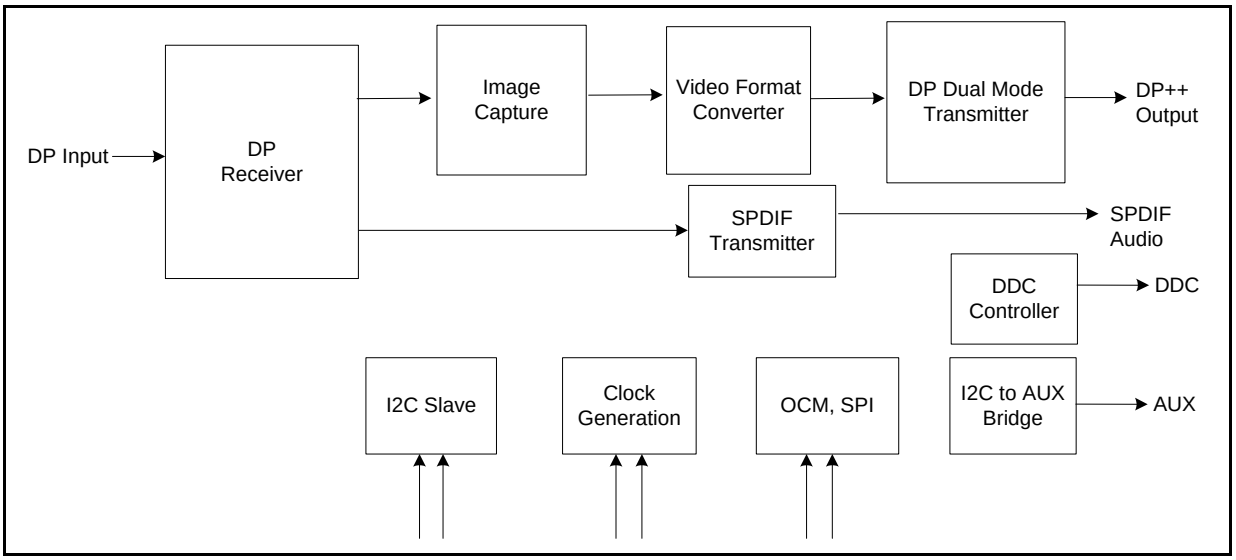
## Features

- DisplayPort® dual-mode transmitter
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - Supports eDP operation
  - HDMI/DVI operation with level translator
- DisplayPort receiver
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - Supports eDP operation
- SPDIF audio output
  - 192 kHz/24 bits
  - Compressed/LPCM
- HDCP repeater with embedded keys
- ASSR - eDP display authentication option
- AUX to I2C bridge for EDID/MCCS pass through
- Spread spectrum on DisplayPort interface for EMI reduction
- Device configuration options
  - SPI Flash
  - I2C host interface
- Deep color support
  - RGB/YCC (4:4:4) – 16-bit color
  - YCC (4:2:2) – 16-bit color
  - Color space conversion – YUV to RGB and RGB to YUV
- Bandwidth
  - Video resolution up to 4K x 2K @ 30 Hz; 1920 x 1080 @ 120 Hz
  - Audio 7.1 Ch up to 192 kHz sample rate
- Low power operation; active 493 mW, standby 21 mW
- Package
  - 81 BGA (8 x 8 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

## Applications

- Audio-video accessory (dongle) for PC/notebooks and docking stations
- Thunderbolt source and peripheral devices


DP Input
DP Receiver
Image Capture
Video Format Converter
DP Dual Mode Transmitter
DP++ Output
SPDIF Transmitter
SPDIF Audio
DDC Controller
DDC
I2C Slave
Clock Generation
OCM, SPI
I2C to AUX Bridge
AUX

# 1. Description

The STDP2690 is a high-speed DisplayPort to DisplayPort dual mode converter IC targeted for applications such as audio-video accessories, docking stations, Thunderbolt storage devices, etc. This device includes a VESA DP Standard Ver. 1.2a compliant receiver and transmitter, implementing single link DisplayPort input and output ports comprising four Main lanes, AUX CH, and HPD.

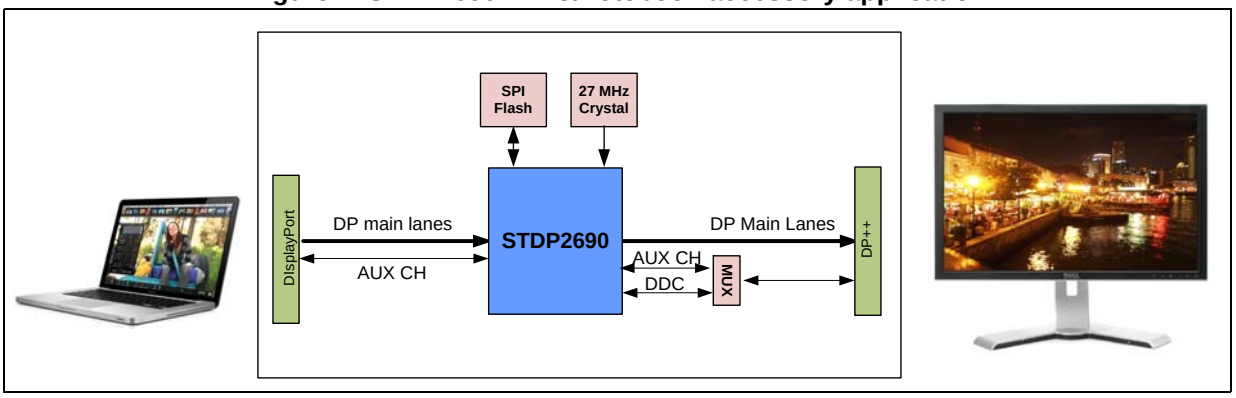
The STDP2690 uses MegaChips' latest generation DisplayPort dual mode transmitter technology that supports both DisplayPort and TMDS signal formats (DP++). DisplayPort receiver and transmitter support HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. The transmitter is capable of supporting HDMI or single link DVI output through a passive level translator (dongle). When configured as HDMI output, this device supports link rate up to 2.97 Gbps that corresponds to a pixel rate of 297 MHz, adequate for handling video timings up to FHD 120 Hz 3D formats. This device delivers deep color video up to 16-bits per color at 1080p 60 Hz and lower video resolutions. The STDP2690 allows audio transport from the source to desired audio rendering devices over the DP++ output or through the SPDIF port. The audio signal from the source can be routed simultaneously to DP++ and SPDIF output ports. For example, the STDP2690 allows routing of any two audio channels on the SPDIF port, while transporting up to eight channels on the DP++ port.

The STDP2690 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. This device features HDCP 1.3 content protection scheme with an embedded key option for secure transmission of digital audio-video content. It also operates as an HDCP repeater for the downstream sink. The eDP authentication option ASSR (Alternative Scrambler Seed Reset) is supported for embedded application.

The AUX-to-I2C translator in the STDP2690 allows the upstream DisplayPort source to access EDID and transfer MCCS commands to a downstream sink over the HDMI interface when used with a level translator. This device has an on-chip microcontroller with SPI and I2C host interface for system configuration purposes. STDP2690 can be configured with an external SPI Flash for custom applications. In addition, it allows register level configuration from an external host controller through I2C interface.

# 2. Application overview

**Figure 1. STDP2690 in PC/notebook accessory application**



# 3. Feature attributes

## 3.1 Input interface

- DP standard Ver. 1.2a compliant
- Main link configuration (SST format only, no MST format support)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: 1 Mbps Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB or YCC422 or YcC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates

## 3.2 Output interface

- DP++ transmitter interface featuring
  - AC coupled DisplayPort Ver. 1.2a interface
  - AC coupled HDMI 1.4 interface to external level translators
- DP main link configuration (SST format only, no MST format support)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB or YCC422 or YcC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 2.97 Gbps/data pair max

## 3.3 Deep color support

- RGB/YCC (4:4:4) – 16-bit color
- YCC (4:2:2) – 16-bit color
- Color space conversion – YUV to RGB and RGB to YUV

## 3.4 Supported video timings

- 4096 x 2160 (4K x 2K) 60 Hz: 24 bits/pixel (DP to DP only)
- 4096 x 2160 (4K x 2K) 24 Hz/30 Hz: 24 bits/pixel (DP to HDMI)
- 1920 x 1080 (FHD) 120 Hz: 24 bits/pixel
- 2560 x 1600 (WQXGA) 60 Hz: 24 bits/pixel
- Up to 1920 x 1080 (FHD) 60 Hz, 48, 36, 30 bits/pixel
- All compatible 3D formats defined in DP 1.2a and HDMI 1.4 specifications
- All standard CEA861 timing formats

## 3.5 Supported audio timings

- All audio formats as specified in DP 1.2a and HDMI 1.4 specifications
- SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz

## 3.6 Control channel interfaces

- AUX CH, I2C host interface, SPI (optional), and UART (UART for test/debug purposes only)

## 3.7 HDCP 1.3 support

- Key sets for DP RX and DP/HDMI TX integrated in one-time programmable ROM (OTP)
- Standalone HDCP repeater capability
- Supports eDP display authentication option ASSR (Alternate Scrambler Seed Reset)

## 3.8 Package

- 81 BGA (8 x 8 mm), 0.8 ball pitch

## 3.9 Power supply voltages

- 3.3 V I/O; 1.2 V core

## 3.10 ESD

- 2 KV HBM, 500 V CDM

# 4. Ordering information

**Table 1. Order codes**

| Part number | Description |
|---|---|
| STDP2690-AD | 81 BGA (8 x 8 mm) delivered in trays |
| STDP2690-ADT | 81 BGA (8 x 8 mm) delivered in tape and reel |

# 5. Revision history

**Table 2. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Jun-2012 | 1 | Initial release. |
| 07-May-2013 | 2 | Changed DP1.2 to DP1.2a throughout.<br>Added eDP and ASSR feature in first page Features, Description, and Feature attribute sections.<br>Updated Ordering information section. |
| 22-May-2014 | 3 | Updated to comply with MegaChips documentation style/formatting. |
| 15-Sep-2014 | 4 | Updated footers and added copyright information to last page. |

## Notice

Semiconductor products may possibly experience breakdown or malfunction. Adequate care should be taken with respect to the safety design of equipment in order to prevent the occurrence of human injury, fire or social loss in the event of breakdown or malfunction of semiconductor products

The overview of operations and illustration of applications described in this document indicate the conceptual method of use of the semiconductor product and do not guarantee operability in equipment in which the product is actually used.

The names of companies and trademarks stated in this document are registered trademarks of the relevant companies.

MegaChips Co. provides no guarantees nor grants any implementation rights with respect to industrial property rights, intellectual property rights and other such rights belonging to third parties or/and MegaChips Co. in the use of products and of technical information including information on the overview of operations and the circuit diagrams that are described in this document.

The product described in this document may possibly be considered goods or technology regulated by the Foreign Currency and Foreign Trade Control Law. In the event such law applies, export license will be required under said law when exporting the product. This regulation shall be valid in Japan domestic.

In the event the intention is to use the product described in this document in applications that require an extremely high standard of reliability such as nuclear systems, aerospace equipment or medical equipment for life support, please contact the sales department of MegaChips Co. in advance.

All information contained in this document is subject to change without notice.



MegaChips Corporation
Head Quarters
1-1-1 Miyahara, Yodogawa-ku Osaka 532-0003, Japan
TEL: +81-6-6399-2884

MegaChips Corporation
Tokyo Office
17-6 Ichiban-cho, Chiyoda-ku, Tokyo 102-0082, Japan
TEL: +81-3-3512-5080

MegaChips Corporation
Makuhari Office
1-3 Nakase Mihama-ku Chiba 261-8501, Japan
TEL: +81-43-296-7414

MegaChips Corporation
San Jose Office
2033 Gateway Place, Suite 400, San Jose, CA 95110 U.S.A.
TEL: +1-408-570-0555

MegaChips Corporation
India Branch
17th Floor, Concorde Block UB City,
Vittal Mallya Road, Bangalore 560-001, India
TEL: +91-80-4041-3999

MegaChips Corporation
Taiwan Branch
RM. B 2F, Worldwide House, No.129,
Min Sheng E. Rd., Sec. 3, Taipei 105, Taiwan
TEL: +886-2-2547-1297

MegaChips Corporation
Tainan Office
RM. 2, 8F, No.24, Da Qiao 2 Rd., Yong Kang Dist.,
Tainan 710, Taiwan
TEL: +886-6-302-2898

MegaChips Corporation
Zhunan Office
No.118, Chung-Hua Rd., Chu-Nan, Miao-Li 350, Taiwan
TEL: +886-37-666-156

MegaChips Corporation
Shenzhen Office
Room 6307, Office Tower, Shun Hing Square, 5002
Shen Nan Dong Road, Luohu District,
Shenzhen 518000, P. R. China
TEL: +86-755-3664-6990