LTC2393-16/LTC2392-16/ LTC2391-16: 16-Bit,1Msps/ 0.5Msps/0.25Msps Low Noise ADCs

DESCRIPTION

The LTC®2393/LTC2392/LTC2391-16 are low noise high speed ADCs with both parallel and serial outputs that can operate from a single 5V supply. The following text refers to the LTC2393-16 but applies to all three parts. The only difference being the maximum sample rates. The LTC2393-16 supports a large ±4.096V fully differential input range. This makes it ideal for high performance applications that require maximum dynamic range. Demonstration circuit 1500A provides the user a means of evaluating the performance of the LTC2393-16 in both parallel and serial modes and is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. Also several suggested driver circuits for the analog inputs will be presented.

Design files for this circuit board are available at www.linear.com/demo.

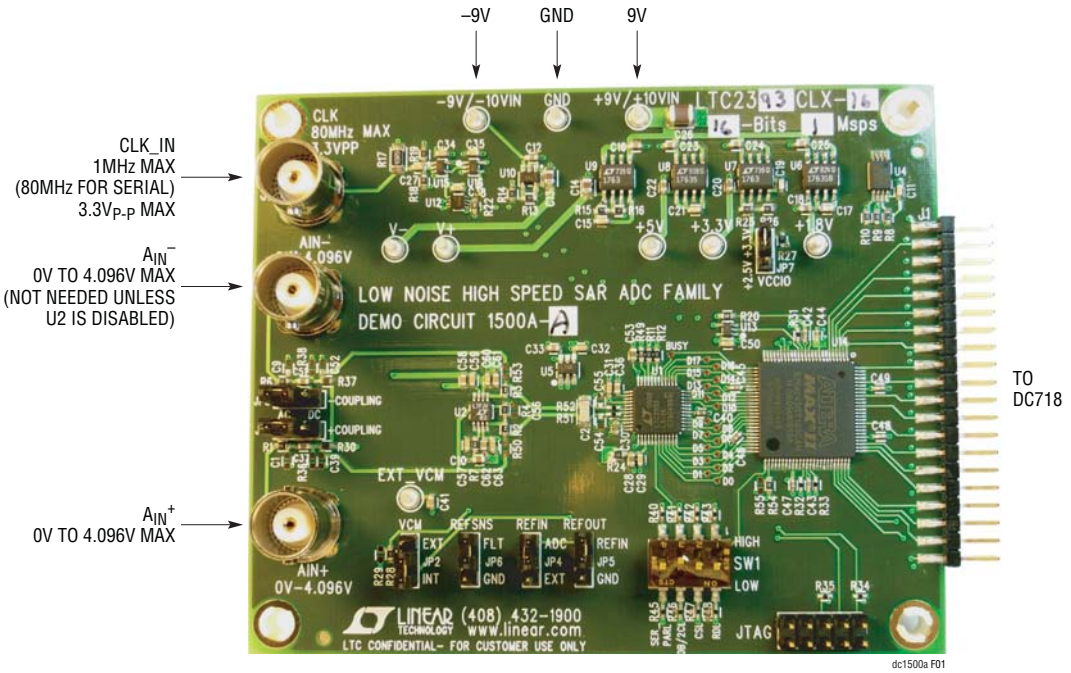


Figure 1. DC1500A Connection Diagram

Table 1

ASSEMBLY VERSION	PART NUMBER	MAX CONVERSION RATE	MAX PARALLEL CLK IN FREQUENCY	MAX SERIAL CLK IN FREQUENCY
DC1500A-A	LTC2393CLX-16	1Msps	1MHz	80MHz
DC1500A-B	LTC2392CLX-16	0.5Msps	500kHz	40MHz
DC1500A-C	LTC2391CLX-16	0.25Msps	250kHz	20MHz

QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set as shown in the connection diagram of Figure 1. The default connections configure the ADC for parallel operation with the output data in offset binary format. The analog input is AC-coupled and the internal reference of the ADC is used.

Connect DC1500A to a DC718B/C USB High Speed Data Collection Board using connector J1. Connect DC718B/C to a host PC with a standard USB A/B cable. Apply ±9V to the indicated terminals. Apply a low jitter signal source to J3 (AIN^+). The default setup uses a single ended to differential converter so that it is only necessary to apply an input signal to J3. Connect a low jitter 1MHz $3.3V_{P-P}$ sine wave or square wave to connector J2 (CLK). Note that J2 has a 50Ω termination resistor to ground.

Run the QuickEval-II software (Pscope.exe version K66 or later) supplied with DC718B/C or download it from www.linear.com.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The Pscope software should recognize DC1500A and configure itself automatically.

Click the Collect button (see Figure 6) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

SETUP

DC Power

DC1500A requires ±9VDC at approximately 100mA. Most of the supply current is consumed by the CPLD, op amps, regulators and discreet logic on the board. The ±9VDC input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and op amps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter $3.3V_{P-P}$ sine or square wave to J2. The clock input is AC-coupled so the DC level of the clock signal is not important. A generator like the HP8644 or similar is recommended. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired sample rate. One way to do this is by placing the ADC in the serial mode. This can be accomplished by setting the SER/PARL position of SW1 to the high position. In the serial mode the ratio of clock frequency to conversion rate is 80:1. In the parallel mode there is a 1:1 ratio of clock frequency to conversion rate. If the clock input is to be driven with logic, it is recommended that the 50Ω terminator (R17) be removed. Slow rising edges may compromise SNR of the converter in the presence of high amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 3.3V default), if not connected to DC718, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 3 of J1 to latch the data. The data can be latched using either edge of this signal. The data output signal levels at J1 can also be reduced to 0V to 2.5V if the application circuit cannot tolerate the higher voltage. This is accomplished by moving JP7 to the 2.5V position.

Reference

JP4, JP5 and JP6 allow you to select an on chip reference or an external LT1790A-4.096 as the reference. The worst case initial accuracy and drift specifications of the external reference are better than the on chip reference. To use the internal reference set JP6 to FLT, JP4 to ADC and JP5 to REFIN. To use the LT1790A-4.096 set JP5 and JP6 to GND and JP4 to EXT.

SETUP

Analog Input

The default driver for the analog inputs of the LTC2393-16 on DC1500A is shown in Figure 2. This circuit converts a single-ended 0V to 4.096V input signal applied at A_{IN} into a differential signal with a swing of ±4.096V between the +IN and –IN inputs of the ADC. In addition this circuit band limits the input frequencies to approximately 100kHz which is the useful linear bandwidth of the LTC2393-16.

Alternatively, if your application circuit produces a differential signal which can drive the ADC but you need to level shift the input signal, the circuits of Figure 3 and Figure 4 can be used. The circuit of Figure 3 AC-couples the input signal and is usable down to about 10kHz. The lower frequency limit can be extended by increasing C37 and C51. The circuit of Figure 3 can be implemented on DC1500A by putting JP1 and JP3 in the AC position and moving R2 and R3 to the R50 and R53 positions. At this point it will be necessary to drive both A_{IN}^+ and A_{IN}^-. One of these RC pairs can be attached to the input of the circuit in Figure 2. This allows a single-ended input signal to be level shifted. This is the default condition for DC1500A. One of the most asked for ADC driver circuits is one that allows the input voltage to go below ground with a single supply ADC. Figure 4's input driver allows the input voltage range to go below ground. It DC-couples and level shifts the analog input at the expense of attenuating the input level by a factor of 2. The circuit of Figure 4 can be implemented on DC1500A by setting V_{CM} to External and biasing the external pin to 4.096V. Then replace R1 and R6 with 1k, put JP1 and JP3 in the DC position and move R2 and R3 to the R50 and R53 positions.

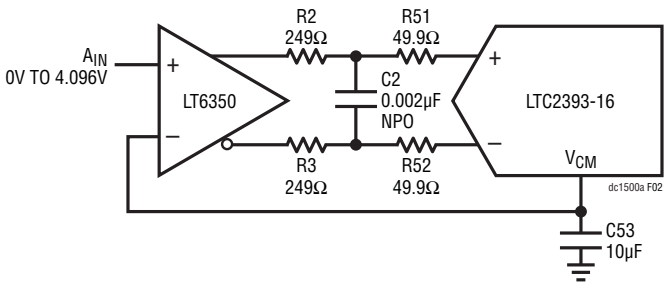


Figure 2. Single-Ended to Differential Driver

Data Collection

For SINAD, THD or SNR testing a low noise, low distortion generator such as the B&K Type 1051 or Stanford Research DS360 should be used. A low jitter RF oscillator such as the HP8644 is used as the clock source.

This demo board is tested in house by attempting to duplicate the FFT plot shown on the front page of the LTC2393-16 data sheet. This involves using a 1MHz clock source, along with a sinusoidal generator at a frequency of 20kHz. The input signal level is approximately –1dBfs. The input is filtered with a 20kHz single pole RC filter shown in Figure 5. The FFT shown in the data sheet is a 16384-point FFT. A typical FFT obtained with DC1500A is shown in Figure 6. Note that to calculate the real SNR, the signal level (F1 amplitude = –1.117dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 6, this means that the actual SNR would be 94.237dB instead of the 93.12dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 93.68 dB which is fairly close to the typical value for this ADC.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm levels of frequency accuracy or if it cannot be slaved to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

SETUP

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on DC1500A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2393-16. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2393-16, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, which can reduce distortion NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2393-16 should have low distortion, low noise and a fast settling time such as the LT6350.

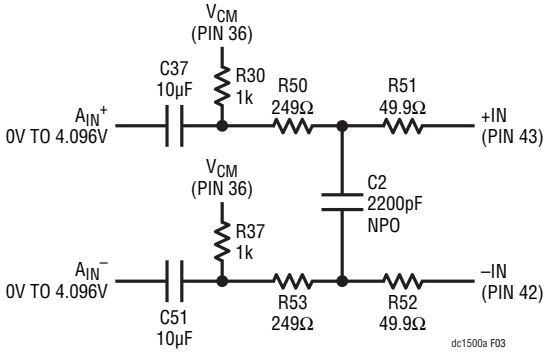


Figure 3. AC-Coupled Differential Driver

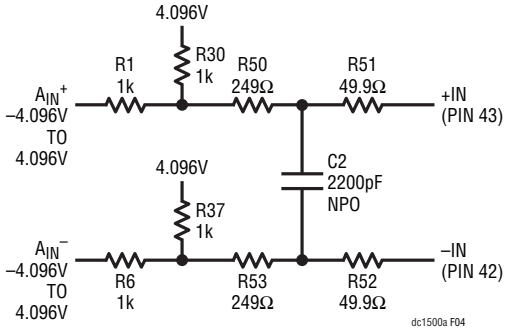


Figure 4. DC-Coupled Differential Driver

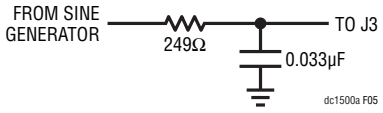


Figure 5. 20kHz RC Filter

SETUP

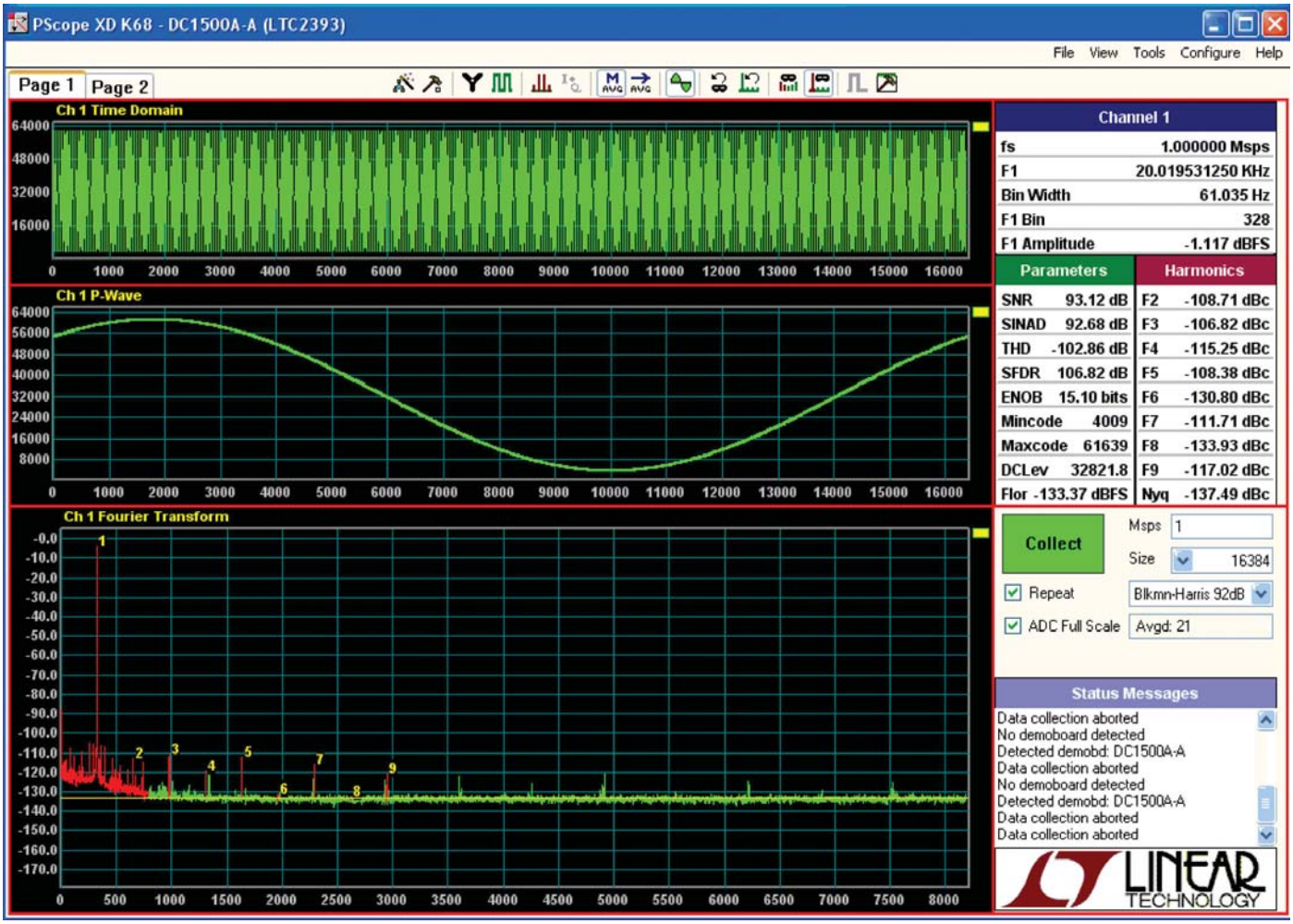


Figure 6. Pscope Screenshot

MISCELLANEOUS DIP SWITCHES AND JUMPERS

Definitions

JP2: V_{CM} sets the DC bias for A_{IN}^+ and A_{IN}^- when the inputs are AC-coupled. INT is the default position.

SW1:

SER_PARL: Selects serial or parallel operation. Default position is parallel. In parallel mode $f_S = f_{CLK}$. In serial mode $f_S = f_{CLK}/80$.

OB/2CL: Selects offset binary or two's complement data format for ADC output word. The default is offset binary.

CSL: This pin must be kept low for normal operation.

RDL: This pin must be kept low for normal operation.

PARTS LIST

LTC23xxCLX Family, DC1500A-1 General BOM

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
1	0	C1, C9, C39, C52, C54, C55, C56	Capacitor, 0603	OPT
2	1	C2	Capacitor, NP0, 2200pF, 25V, 5% 1206	AVX, 12063A222JAT2A
3	9	C10, C18, C20, C22, C28, C30, C37, C51, C53	Capacitor, X5R, 10µF, 6.3V, 20% 0603	Taiyo Yuden, JMK107BJ106MA (2rls, PbF)
4	13	C11, C27, C29, C31, C32, C34, C35, C38, C50, C57, C59, C60, C63	Capacitor, X7R, 0.1µF, 25V, 10% 0603	AVX, 06033C104KAT2A
5	11	C12, C16, C23, C24, C25, C33, C36, C41, C58, C61, C62	Capacitor, X7R, 1µF, 16V, 10% 0603	AVX, 0603YC105KAT2A
6	2	C13, C14	Capacitor, X5R, 10µF, 10V, 20% 0805	Taiyo Yuden, LMK212BJ106MG
7	4	C15, C17, C19, C21	Capacitor, X7R, 0.01µF, 50V, 10% 0603	AVX, 06035C103KAT2A
8	1	C26	Capacitor, X5R, 47µF, 16V, 20% 1210	Taiyo Yuden, EMK325BJ476MM
9	1	C40	Capacitor, X5R, 4.7µF, 4V, 20% 0402	Taiyo Yuden, AMK105BJ475MV-F
10	8	C42, C43, C44, C45, C46, C47, C48, C49	Capacitor, X5R, 0.1µF, 10V, 10% 0402	AVX, 0402ZD104KAT2A
11	9	E1, E2, E3, E4, E5, E6, E7, E8, E9	Test Point, Turret, .064"	Mill-Max, 2308-2-00-80-00-00-07-0
12	6	JP1, JP2, JP3, JP4, JP5, JP6	JMP, 1 × 3, 0.1"	Samtec, TSW-103-07-L-S
13	6	Shunts On JP1 to JP6 Pins 1 and 2	Shunt, 0.1" Center	Samtec, SNT-100-BK-G
14	1	JP7	JMP, 1 × 3, 0.079CC	Samtec, TMM-103-02-L-S
15	1	Shunt On JP7 Pins 1 and 2	Shunt, 0.079" Center	Samtec, 2SN-BK-G
16	1	JTAG	Header, 2 × 5, 0.1"	Samtec, TSW-105-07-L-D
17	1	J1	Header, 0.1 × 0.1 CNTRS, 40 Pin	Samtec, TSW-120-07-L-S
18	3	J2, J3, J4	Connection, BNC, 5 Pins	Connex, 112404
19	3	R1, R4, R6	Resistor, Chip, 0Ω, 1/10W, 0603	Vishay, CRCW06030000Z0EA
20	2	R2, R3	Resistor, Chip, 249Ω, 1/10W, 1% 0603	Vishay, CRCW0603249RFKEA
21	1	R7	Resistor, Chip, 499Ω, 1/10W, 1% 0603	Vishay, CRCW0603499RFKEA
22	3	R8, R9, R10	Resistor, Chip, 4.99k, 1/10W, 1% 0603	Vishay, CRCW06034K99FKEA
23	9	R11, R12, R14, R16, R18, R19, R28, R30, R37	Resistor, Chip, 1k, 1/10W, 5% 0603	Vishay, CRCW06031K00JNEA
24	2	R13, R15	Resistor, Chip, 3.92k, 1/10W, 1% 0603	Vishay, CRCW06033K92FKEA
25	1	R17	Resistor, Chip, 49.9Ω, 1/4W, 1% 1206	Vishay, CRCW120649R9FKEA
26	3	R20, R22, R49	Resistor, Chip, 33Ω, 1/10W, 5% 0603	Vishay, CRCW060333R0JNEA
27	1	R24	Resistor, Chip, 1Ω, 1/10W, 5% 0603	Vishay, CRCW06031R00JNEA
28	1	R25	Resistor, Chip, 1.69k, 1/10W, 1% 0603	Vishay, CRCW06031K69FKEA
29	1	R26	Resistor, Chip, 1.54k, 1/10W, 1% 0603	Vishay, CRCW06031K54FKEA
30	1	R27	Resistor, Chip, 2.80k, 1/10W, 1% 0603	Vishay, CRCW06032K80FKEA
31	0	R29, R36, R38, R50, R53, R55	Resistor, Chip, 0603	OPT
32	4	R31, R32, R33, R34	Resistor, Chip, 1k, 1/16W, 5% 0402	Vishay, CRCW04021K00JNED
33	5	R35, R40, R41, R42, R43	Resistor, Chip, 10k, 1/16W, 5% 0402	Vishay, CRCW040210K0JNED
34	4	R45, R46, R47, R48	Resistor, Chip, 300Ω, 1/16W, 5% 0402	Vishay, CRCW0402300RJNED
35	2	R51, R52	Resistor, Chip, 49.9Ω, 1/16W, 1% 0402	Vishay, CRCW040249R9FKED
36	1	R54	Resistor, Chip, 10k, 1/10W, 5% 0603	Vishay, CRCW060310K0JNEA

PARTS LIST

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
37	1	SW1	Switch, 219-4MST	CTS Electronic Components, 219-4MST
38	1	U2	IC., LT6350CMS8, MS8	Linear Tech., LT6350CMS8
39	1	U4	IC., 24LC025, TSSOP-8	Microchip, 24LC025-T/ST
40	1	U5	IC., LT1790ACS6-4.096, SOT23-6	Linear Tech., LT1790ACS6-4.096#PBF
41	1	U6	IC., LT1763CS8-1.8, SO8	Linear Tech., LT1763CS8-1.8#PBF
42	2	U7, U9	IC., LT1763CS8, SO8	Linear Tech., LT1763CS8#PBF
43	1	U8	IC., LT1763CS8-5, SO8	Linear Tech., LT1763CS8-5#PBF
44	1	U10	IC., LT1964ES5-SD, SOT23-5	Linear Tech., LT1964ES5-SD#PBF
45	1	U12	IC., NL17SZ74, US8	On Semi., NL17SZ74USG
46	1	U13	IC., NC7ST04P5X, SC70-5t	Fairchild, NC7ST04P5X
47	1	U14	IC., EPM240GT100C5N, TQFP100	Altera Corp., EPM240GT100C5N
48	1	U15	IC., NC7SZ04P5X, SC70-5	Fairchild, NC7SZ04P5X
49	1	U16	IC., NC7SVU04P5X, SC70-5	Fairchild, NC7SVU04P5X
50	4	Stand-Off at 4 Corners	Stand-Off, Nylon 0.25"	Keystone, 8831(SNAP ON)
51	1		Stencil for Top Side Only	DC1500A-1

LTC2393CLX Family, Demo Circuit 1500A-A

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
1	1	DC1500A-1	General BOM	
2	1	U1	IC., LTC2393CLX-16, LQFP48-7X7	Linear Tech., LTC2393CLX-16#PBF

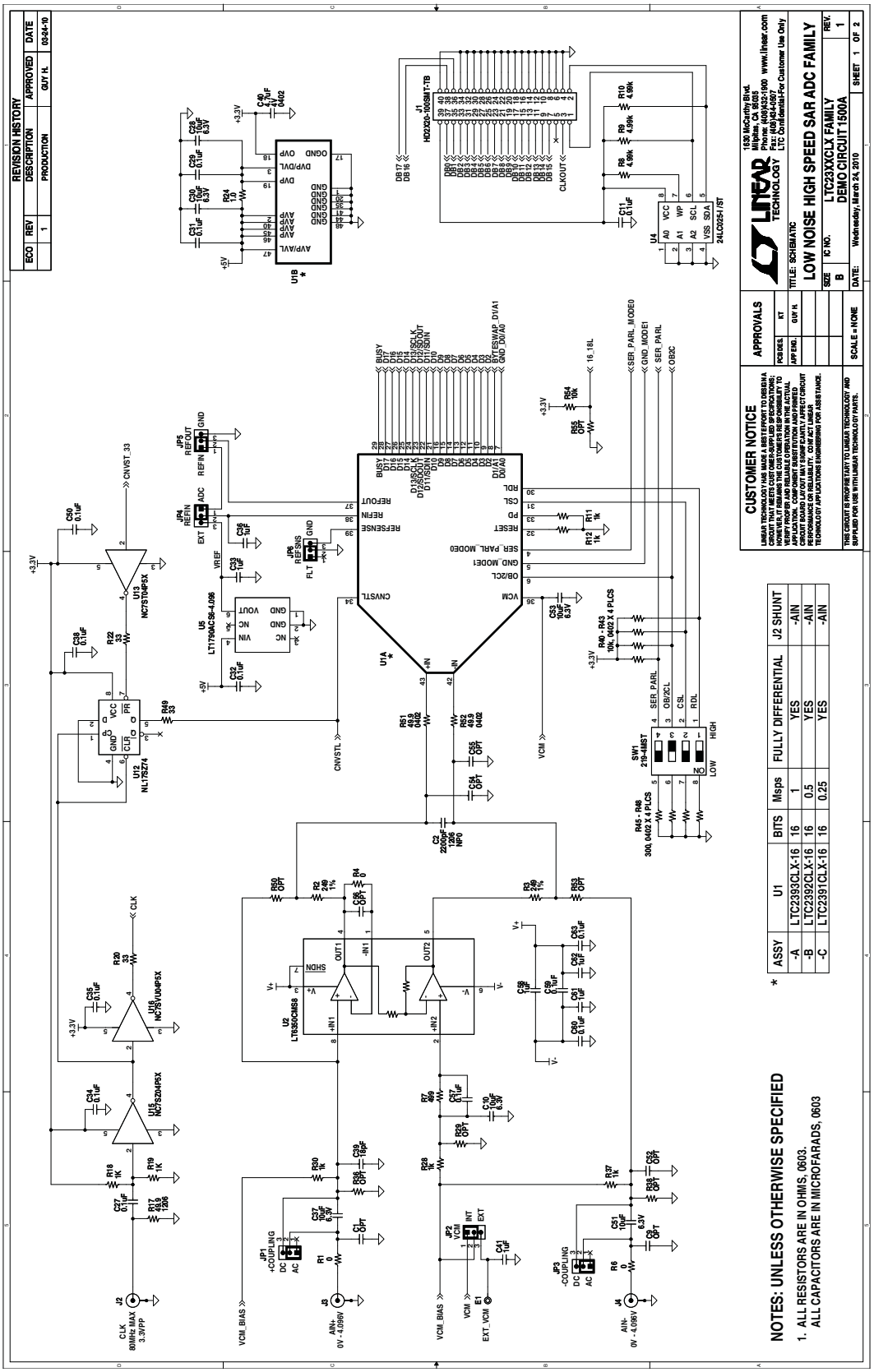
LTC2392CLX-16, Demo Circuit 1500A-B

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
1	1	DC1500A-1	General BOM	
2	1	U1	IC., LTC2392CLX-16, LQFP48-7X7	Linear Tech., LTC2392CLX-16#PBF

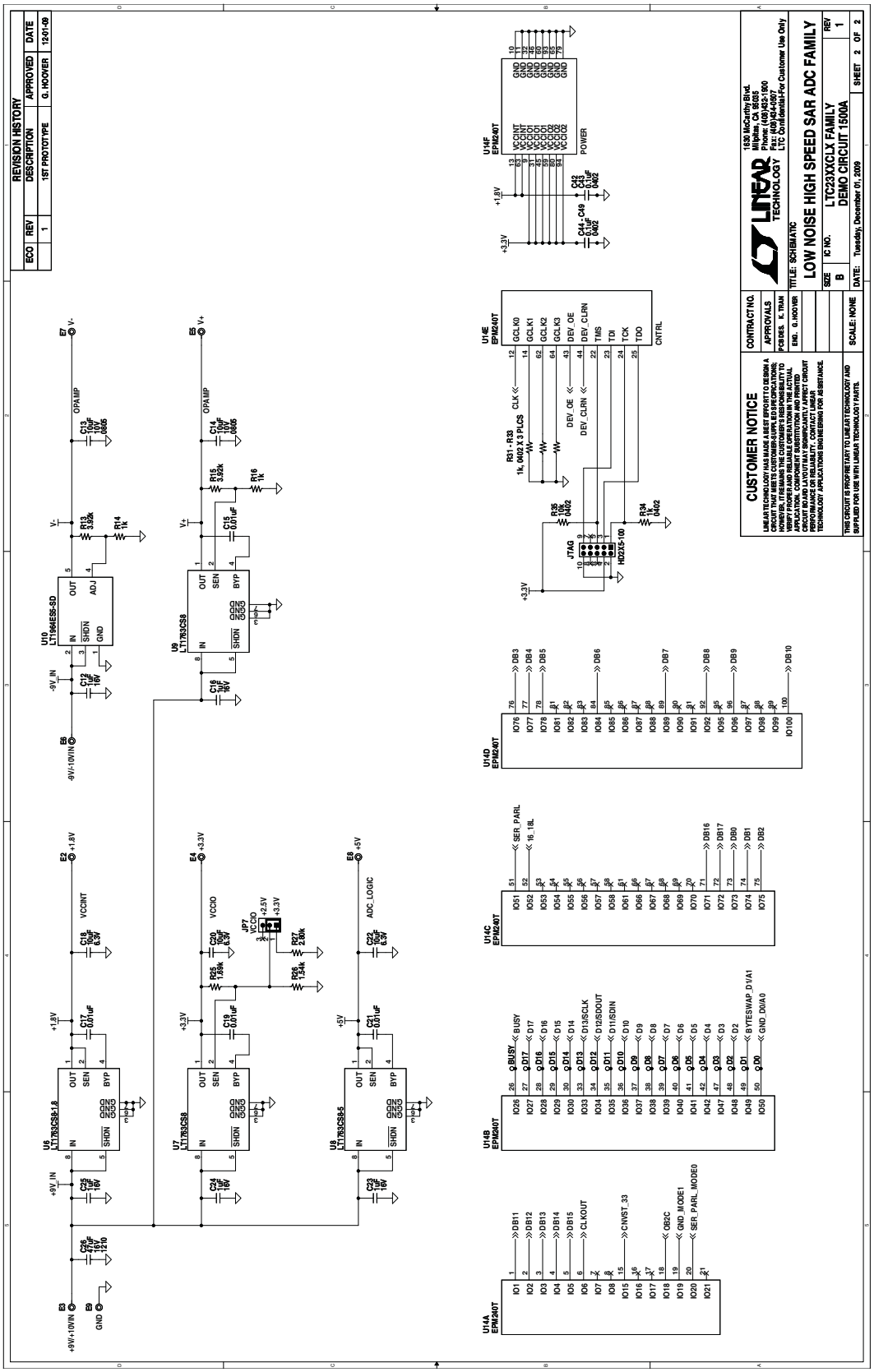
LTC2391CLX-16, Demo Circuit 1500A-C

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
1	1	DC1500A-1	General BOM	
2	1	U1	IC., LTC2391CLX-16, LQFP48-7X7	Linear Tech., LTC2391CLX-16#PBF

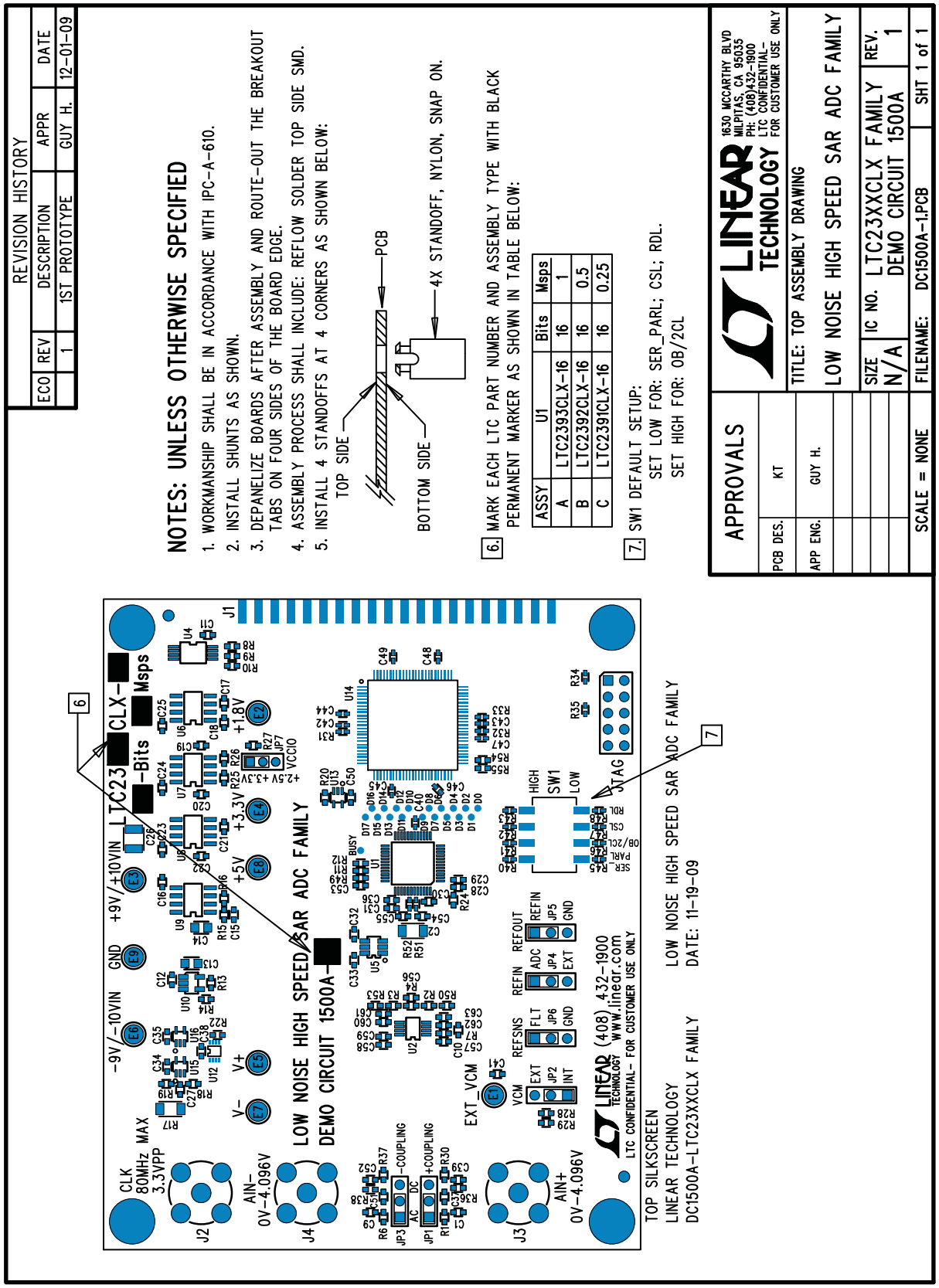
SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM

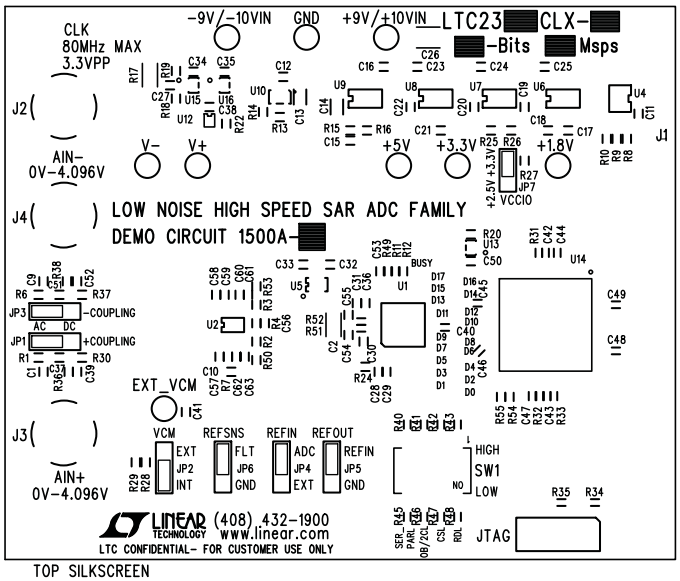


ASSEMBLY DRAWINGS



PCB LAYOUT AND FILM

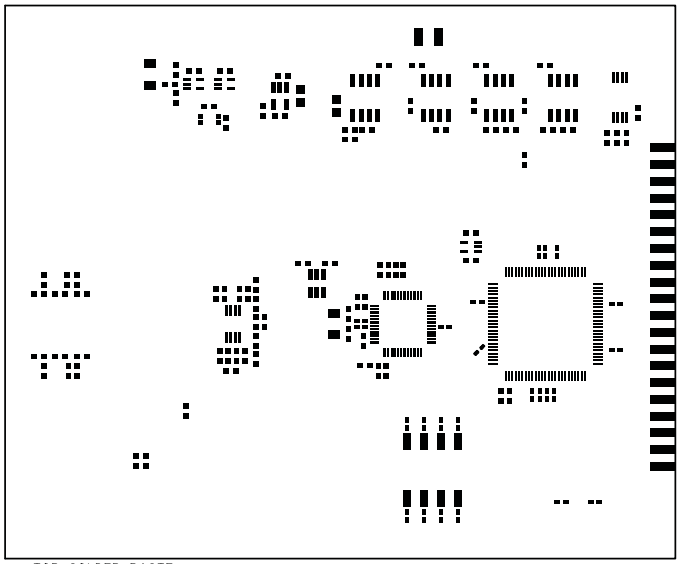
Top Silkscreen



TOP SILKSCREEN
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-19-09

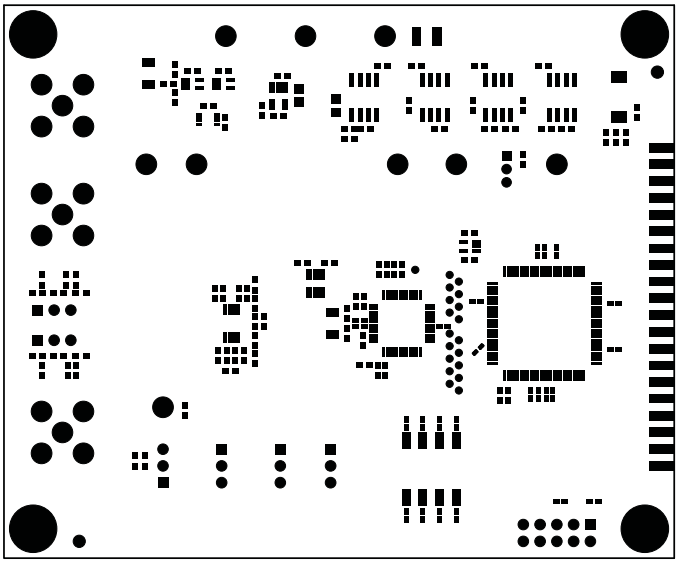
Top Solder Paste



TOP SOLDER PASTE
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

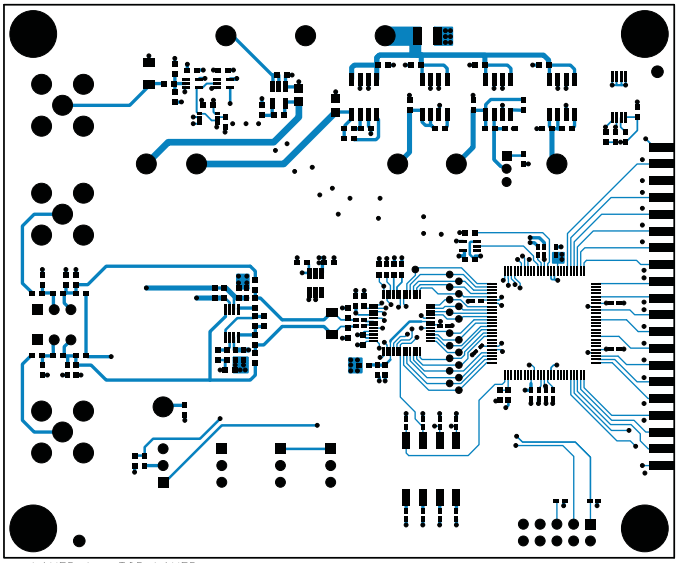
Top Solder Mask



TOP SOLDER MASK
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

Top Layer

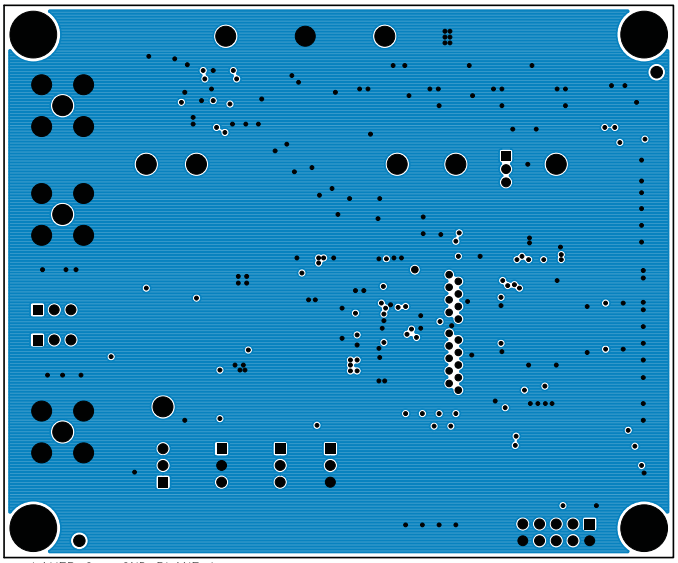


LAYER 1 – TOP LAYER
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

PCB LAYOUT AND FILM

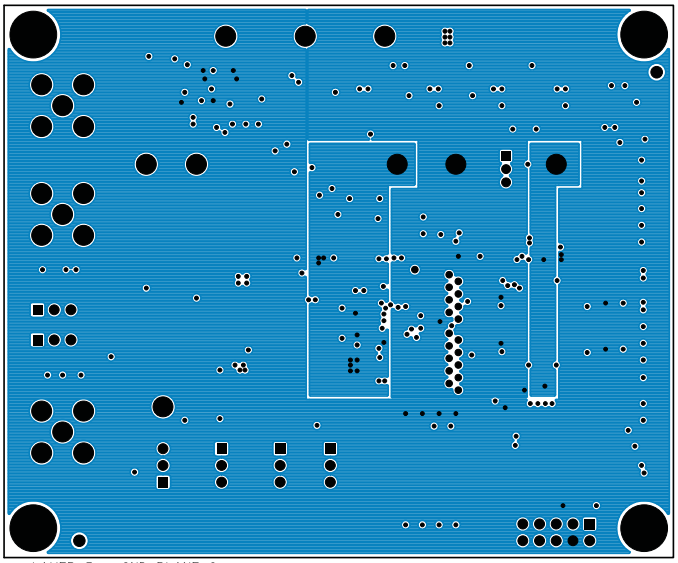
GND Plane 1



LAYER 2 – GND PLANE 1
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

GND Plane 2

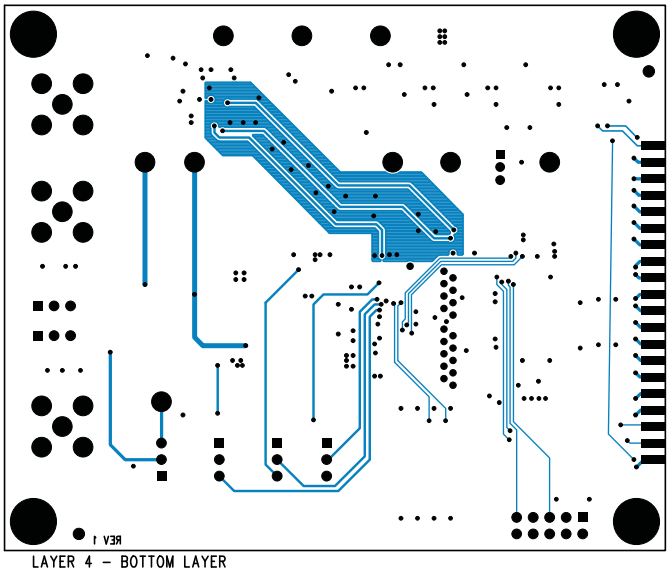


LAYER 3 – GND PLANE 2
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

PCB LAYOUT AND FILM

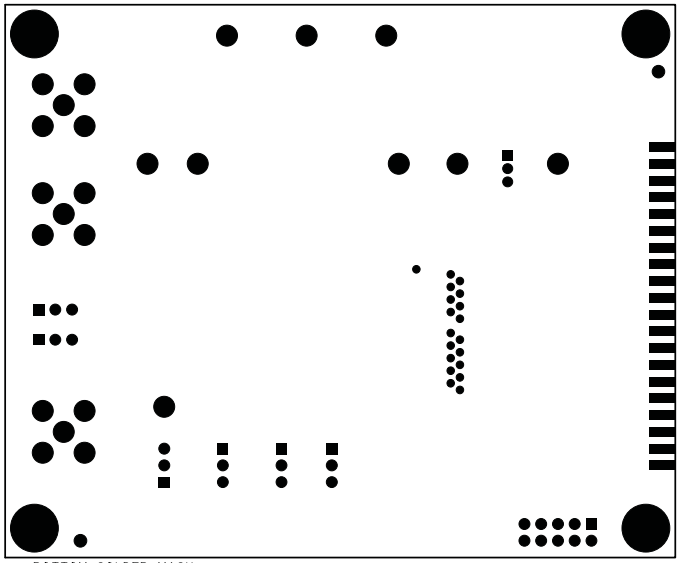
Bottom Layer



LAYER 4 – BOTTOM LAYER
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

Bottom Solder Mask



BOTTOM SOLDER MASK
LINEAR TECHNOLOGY
DC1500A-LTC23XXCLX FAMILY

LOW NOISE HIGH SPEED SAR ADC FAMILY
DATE: 11-02-09

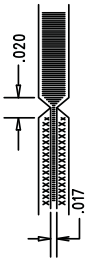
FABRICATION DRAWINGS

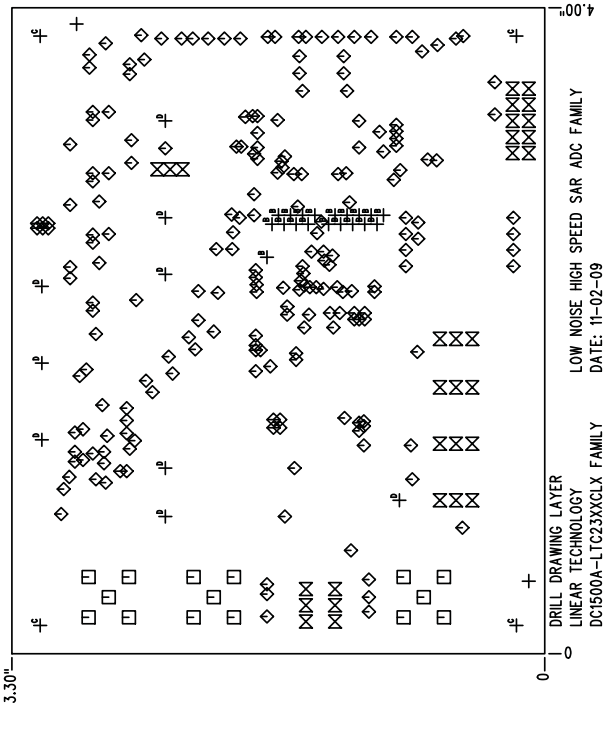
REVISION HISTORY				
ECO	REV	DESCRIPTION	APPR	DATE
	1	1ST PROTOTYPE	G. HOOVER	11-02-09

SIZE	QTY	SYM	PLATED	TOL
0.07	2	+	NO	+/-0.003"
0.055	15	□	YES	+/-0.003"
0.01	214	◇	YES	+/-0.003"
0.035	31	⊠	YES	+/-0.003"
0.02	19	+[B]	YES	+/-0.003"
0.188	4	+[C]	YES	+/-0.003"
0.064	9	+[D]	YES	+/-0.003"

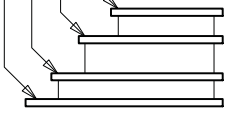
NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -EPOXY FIBERGLASS, NEMA GRADE FR-4
   -FINISHED THICKNESS TO BE 0.062" +/- .005"
   -TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   -FLAMMABILITY RATING: 94 V-0 MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.
4. DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   -ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   -HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
5. FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   -GOLD IMMERSION BOTH SIDES.
   (LEAD FREE SOLDER CAN BE USED FOR PROTOTYPE)
   -FOR SILKSCREEN: BOTH SIDES USE WHITE NON-CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB:





LAYER STRUCTURE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON ANGLE ±1° O.XX = ±0.01" O.XXX = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994

THIRD ANGLE PROJECTION

APPROVALS

	NAME	DATE
PCB DES.	K. TRAN	11-02-09
ENG.	G. HOOVER	11-02-09

LINEAR TECHNOLOGY

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TITLE: FABRICATION DRAWING

LOW NOISE HIGH SPEED SAR ADC FAMILY

SIZE	IC NO.	REV.
A	LTC23XXCLX FAMILY DEMO CIRCUIT 1500A	1

DO NOT SCALE DRAWING	SCALE: NONE	FILENAME: DC1500A.PCB	SHT 1 of 1

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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