

# 8K x 8 Static RAM

## Features

- **High speed**  
— 15 ns
- **Fast  $t_{DOE}$**
- **Low active power**  
— 715 mW
- **Low standby power**  
— 220 mW
- **CMOS for optimum speed/power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

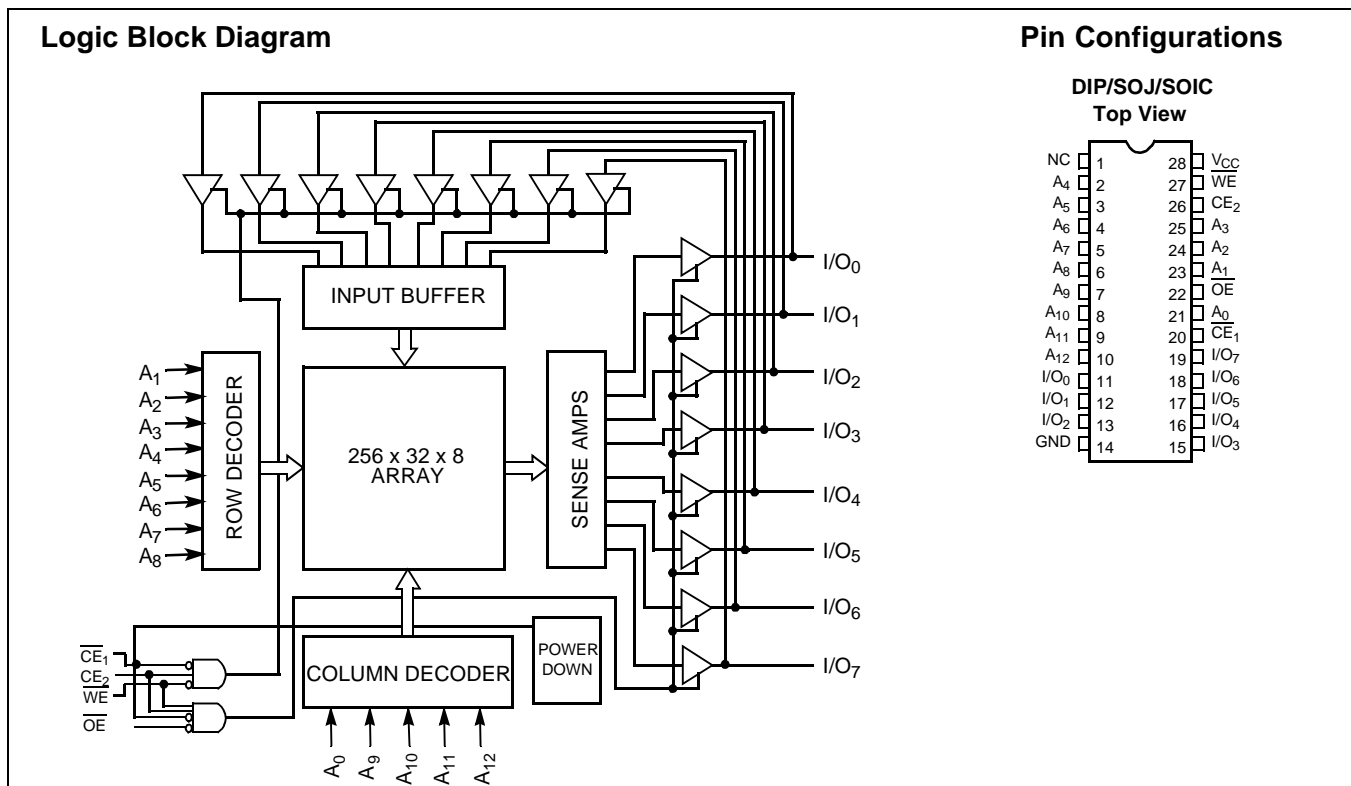
## Functional Description<sup>[1]</sup>

The CY7C185 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is

provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature ( $\overline{CE}_1$  or  $CE_2$ ), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP, SOJ, or SOIC package.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $CE_1$  and  $WE$  inputs are both LOW and  $CE_2$  is HIGH, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{12}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}_1$  and  $\overline{OE}$  active LOW,  $CE_2$  active HIGH, while  $WE$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to insure alpha immunity.



## Selection Guide<sup>[2]</sup>

	7C185-15	7C185-20	7C185-25	7C185-35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)	130	110	100	100
Maximum Standby Current (mA)	40/15	20/15	20/15	20/15

**Note:**

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).
2. For military specifications, see the CY7C185A data sheet.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[3]</sup> ..... -0.5V to +7.0V  
 DC Input Voltage<sup>[3]</sup>..... -0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C185-15		7C185-20		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		130		110	mA
I <sub>SB1</sub>	Automatic Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ or CE <sub>2</sub> ≤ V <sub>IL</sub> Min. Duty Cycle = 100%	40		20		mA
I <sub>SB2</sub>	Automatic Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , or CE <sub>2</sub> ≤ 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	15		15		mA

**Notes:**

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Electrical Characteristics** Over the Operating Range (continued)

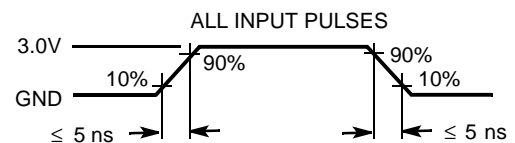
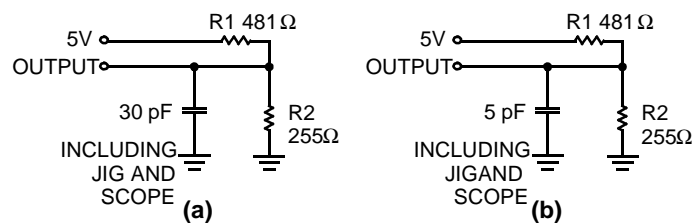
Parameter	Description	Test Conditions	7C185-25		7C185-35		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>oZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		100		100	mA
I <sub>SB1</sub>	Automatic Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ Min. Duty Cycle = 100%		20		20	mA
I <sub>SB2</sub>	Automatic Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		15		15	mA

**Capacitance<sup>[5]</sup>**

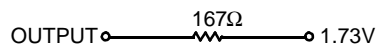
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	7	pF
C <sub>OUT</sub>	Output Capacitance		7	pF

**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT



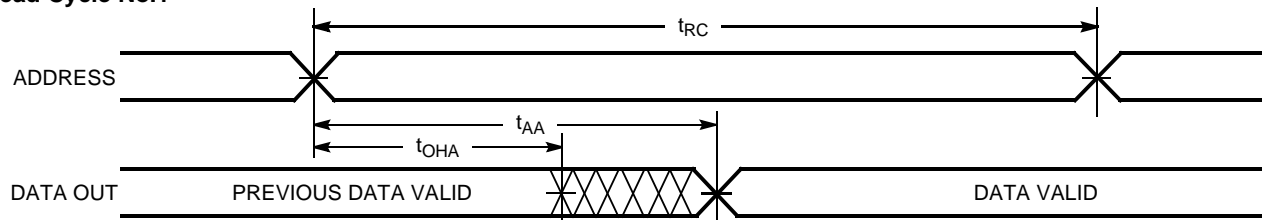
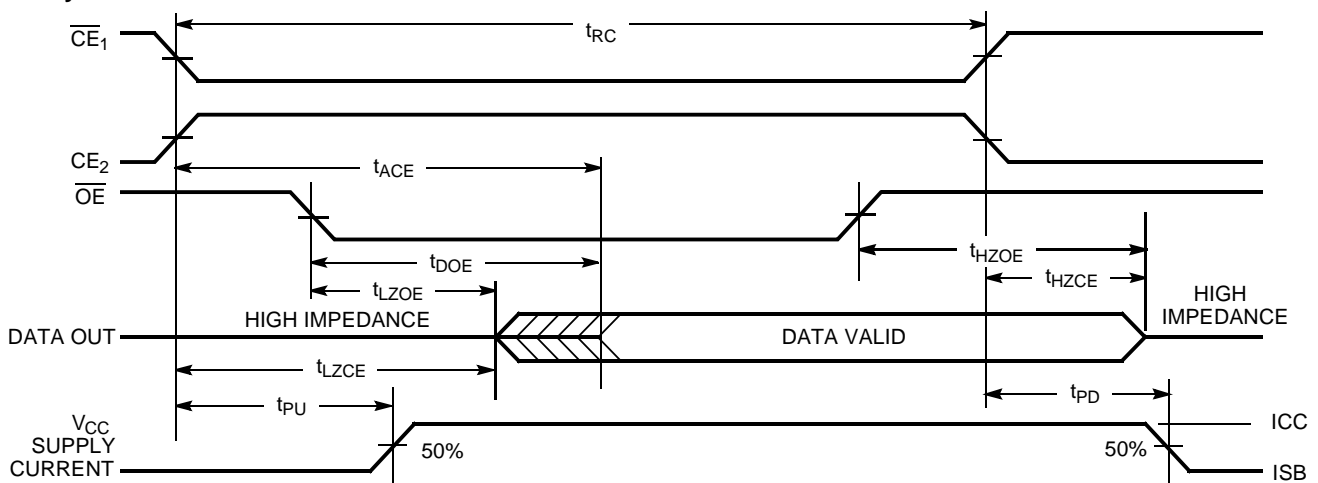
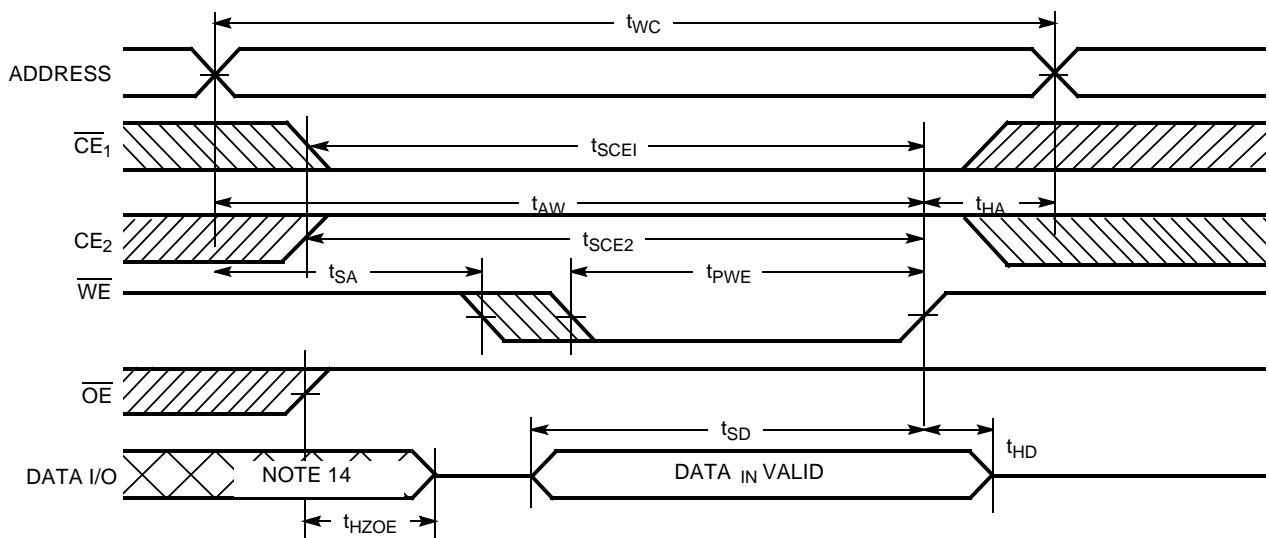
**Switching Characteristics** Over the Operating Range<sup>[6]</sup>

Parameter	Description	7C185-15		7C185-20		7C185-25		7C185-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		15		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		5		5		5		ns
t <sub>ACE1</sub>	$\overline{CE}_1$ LOW to Data Valid		15		20		25		35	ns
t <sub>ACE2</sub>	CE <sub>2</sub> HIGH to Data Valid		15		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		8		9		12		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7]</sup>		7		8		10		10	ns
t <sub>LZCE1</sub>	$\overline{CE}_1$ LOW to Low Z <sup>[8]</sup>	3		5		5		5		ns
t <sub>LZCE2</sub>	CE <sub>2</sub> HIGH to Low Z	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH to High Z <sup>[7, 8]</sup> CE <sub>2</sub> LOW to High Z		7		8		10		10	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW to Power-Up CE <sub>2</sub> to HIGH to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH to Power-Down CE <sub>2</sub> LOW to Power-Down		15		20		20		20	ns
<b>Write Cycle<sup>[9]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	15		20		25		35		ns
t <sub>SCE1</sub>	$\overline{CE}_1$ LOW to Write End	12		15		20		20		ns
t <sub>SCE2</sub>	CE <sub>2</sub> HIGH to Write End	12		15		20		20		ns
t <sub>AW</sub>	Address Set-up to Write End	12		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	12		15		15		20		ns
t <sub>SD</sub>	Data Set-up to Write End	8		10		10		12		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[7]</sup>		7		7		7		8	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns

**Notes:**

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE1</sub> and t<sub>LZCE2</sub> for any given device.
- The internal write time of the memory is defined by the overlap of CE<sub>1</sub> LOW, CE<sub>2</sub> HIGH, and WE LOW. All 3 signals must be active to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Waveforms

**Read Cycle No.1<sup>[10,11]</sup>**

**Read Cycle No.2<sup>[12,13]</sup>**

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[11,13]</sup>**


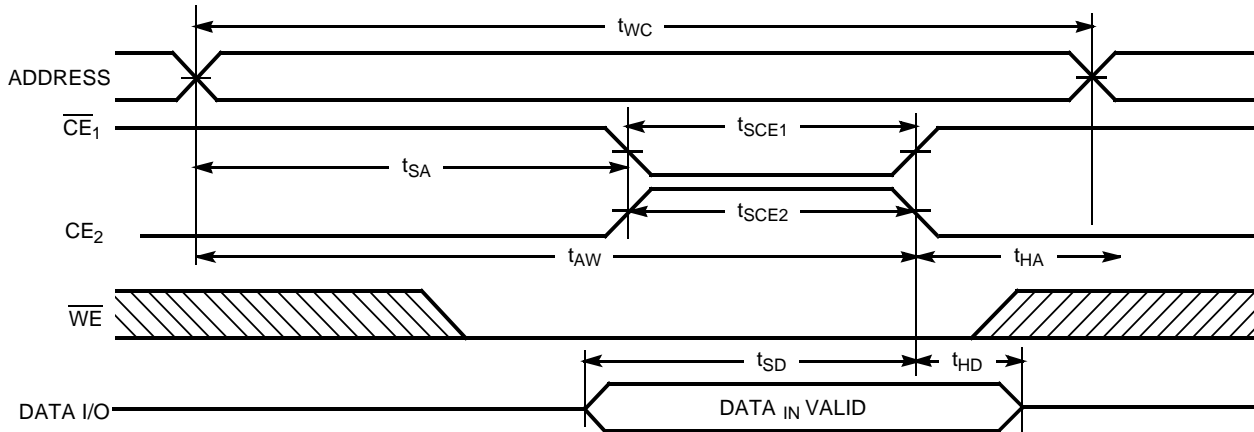
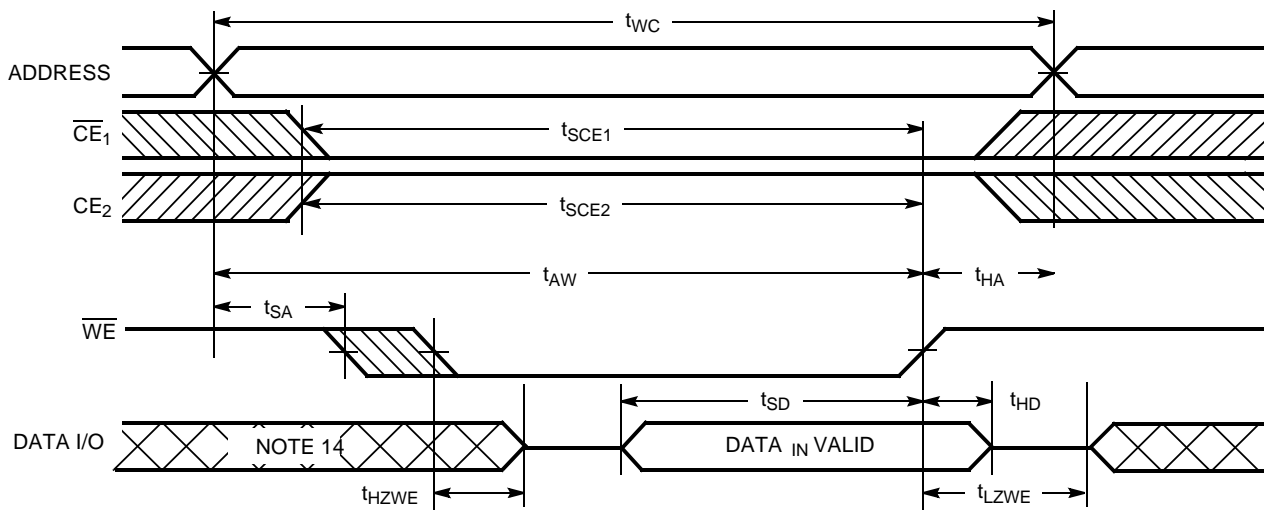
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ .  $\overline{CE}_2 = V_{IH}$ .

11.  $\overline{WE}$  is HIGH for read cycle.

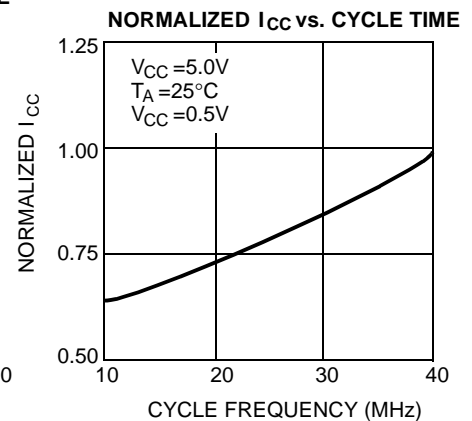
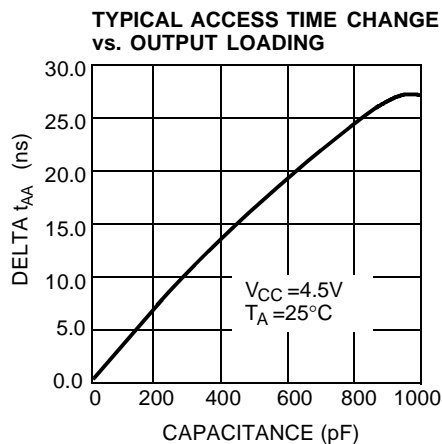
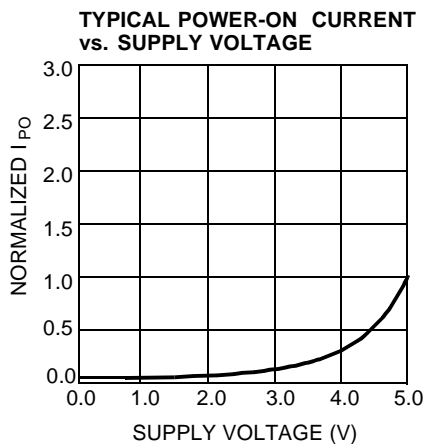
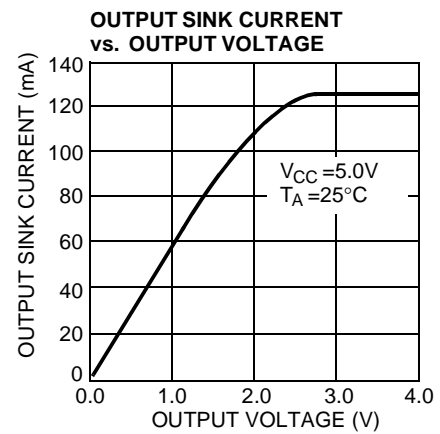
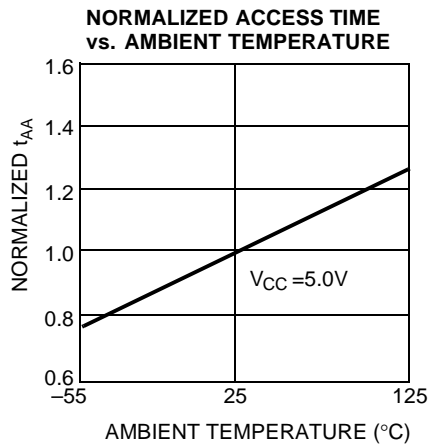
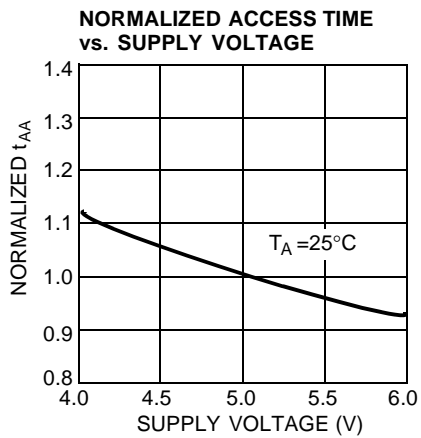
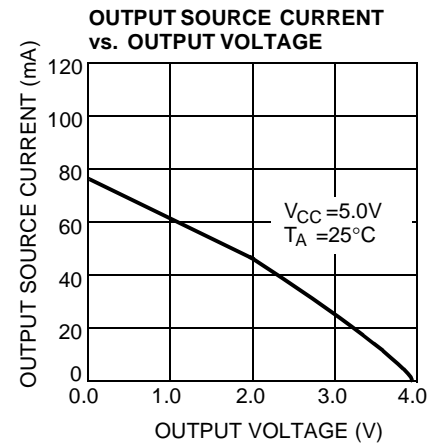
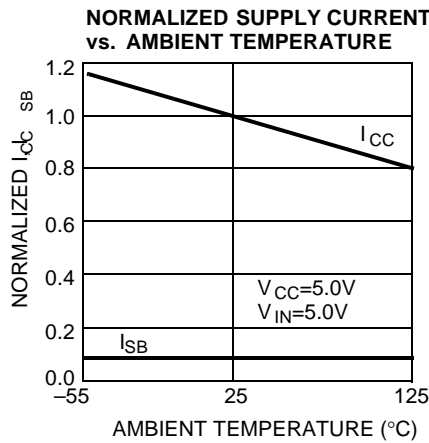
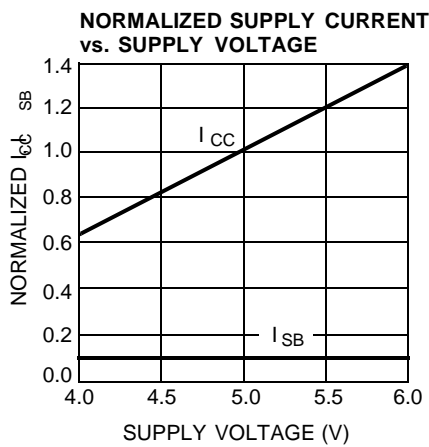
12. Data I/O is High Z if  $\overline{OE} = V_{IH}$ ,  $\overline{CE}_1 = V_{IH}$ ,  $\overline{WE} = V_{IL}$ , or  $\overline{CE}_2 = V_{IL}$ .

13. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $\overline{CE}_2$  must be HIGH to initiate write. A write can be terminated by  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH or  $\overline{CE}_2$  going LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

14. During this period, the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[13,14,15]</sup>**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[13,14,15,16]</sup>**

**Notes:**

15. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
16. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Typical DC and AC Characteristics**


**Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect/Power-Down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

**Address Designators**

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

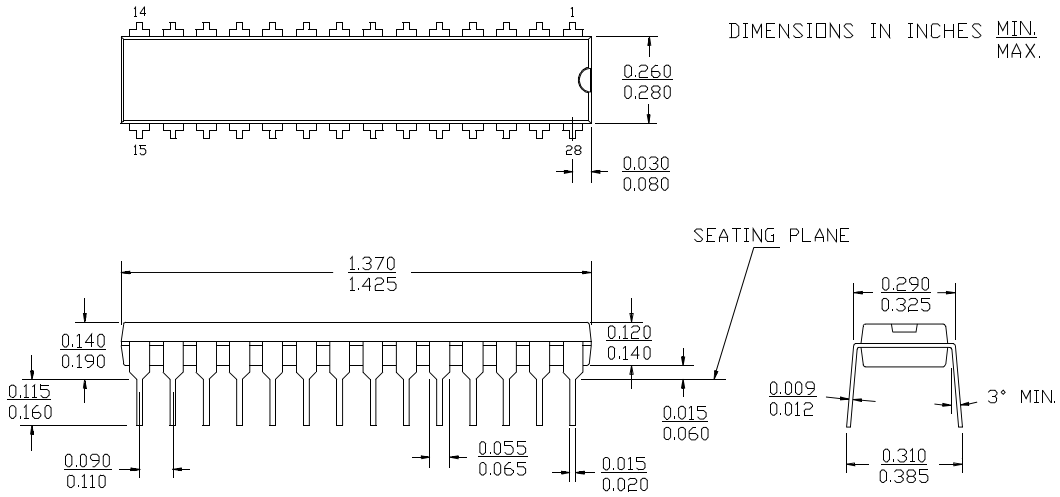
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-15SC	S21	28-Lead Molded SOIC	
	CY7C185-15VC	V21	28-Lead Molded SOJ	
	CY7C185-15VI	V21	28-Lead Molded SOJ	Industrial
20	CY7C185-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-20SC	S21	28-Lead Molded SOIC	
	CY7C185-20VC	V21	28-Lead Molded SOJ	
	CY7C185-20VI	V21	28-Lead Molded SOJ	Industrial
25	CY7C185-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-25SC	S21	28-Lead Molded SOIC	
	CY7C185-25VC	V21	28-Lead Molded SOJ	
	CY7C185-25VI	V21	28-Lead Molded SOJ	Industrial
35	CY7C185-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-35SC	S21	28-Lead Molded SOIC	
	CY7C185-35VC	V21	28-Lead Molded SOJ	
	CY7C185-35VI	V21	28-Lead Molded SOJ	Industrial

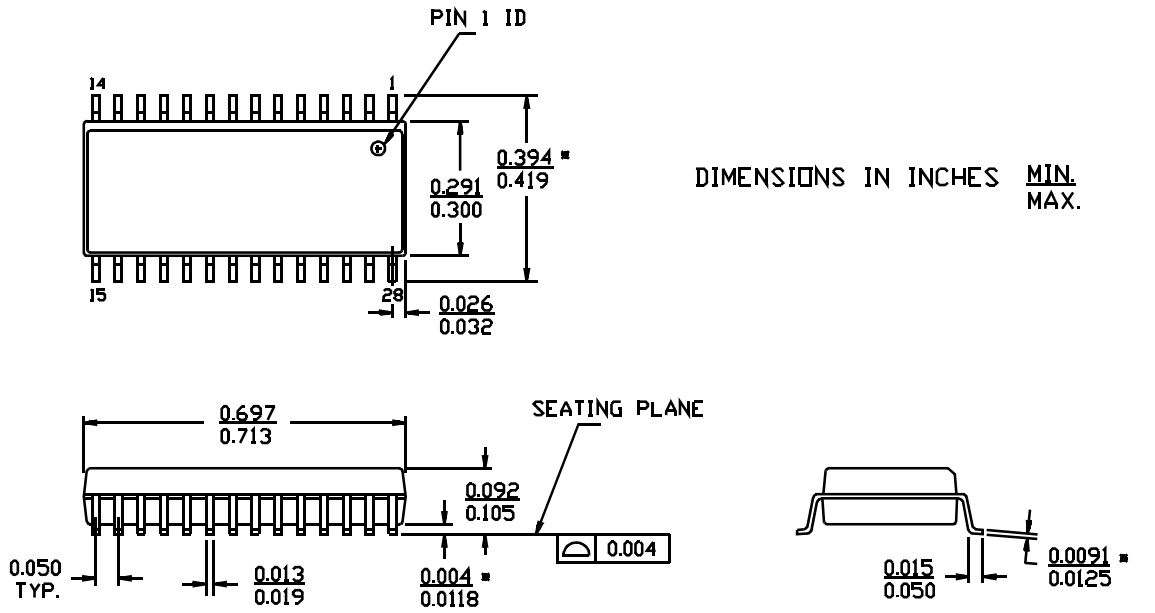


Package Diagrams

28-Lead (300-Mil) Molded DIP P21



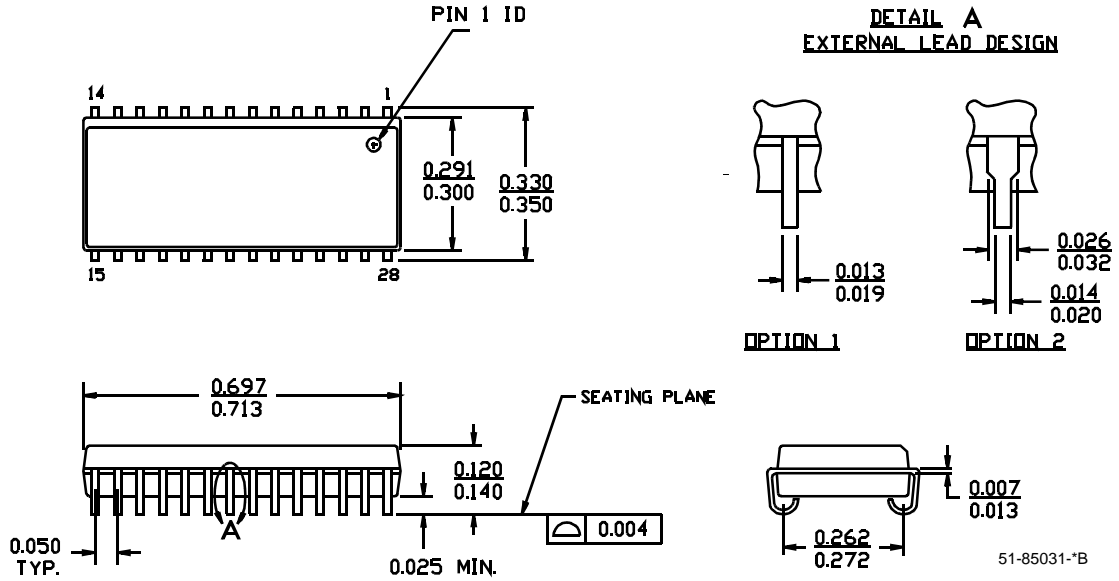
28-Lead (300-Mil) Molded SOIC S21



Package Diagrams (continued)

28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES MIN.  
MAX.



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**Document History Page**

<b>Document Title: CY7C185 8K x 8 Static RAM</b> <b>Document Number: 38-05043</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	107145	09/10/01	SZV	Change from Spec number: 38-00037 to 38-05043
*A	116470	09/16/02	CEA	Add applications foot note to data sheet.