Migration Guide

LTC3880 to LTC3887

INTRODUCTION

The LTC®3887, with the exception of configuration pin resistor values, is a pin-compatible upgrade to the LTC3880. Key features of the LTC3887 vs. LTC3880 include:

- Faster power up time
- All 128 possible PMBus addresses are resistor selectable
- VOUT0 can regulate to 5.5 volts
- PolyPhase® applications can use the differential sense amplifier of channel 0 for improved current sharing
- PolyPhase applications can clock at the desired frequency even if the SYNC pin is not clocking.

This guide describes the differences and explains the configuration file changes needed when migrating a design from the LTC3880 to the LTC3887.

FEATURE COMPARISON

	LTC3880	LTC3887
MFR_ADC_CONTROL for Fast ADC Sampling of a Parameter		✓
PMBus Version	1.1	1.2
Alert Masking (a Part of 1.2 PMBus Compliant)		✓
Shared Differential Sense Amp		✓
Improved SYNC Circuit if Input Clock is Lost		✓
Improved Fault Log Recording		✓
Selectable Number of Addresses with Resistors	16	128
Selectable Number of Output Voltages per Channel with Resistors	256	16
Supports PWM Burst Mode® Operation	✓	

PIN CONFIGURATION

All pins of the LTC3887 except resistor configuration pins are fully compatible with the LTC3880. In most cases, the LTC3887 will work as a drop in replacement of the LTC3880. If the resistor configuration pins are used, resistor configuration values will change and some of the output voltages may not be selectable with the LTC3887. However if the LTC3880 application only uses ASEL resistors, the same LTC3880 circuit and BOM will function identically with the LTC3887.

Specifically for the configuration pins:

- The LTC3887 has two address selection pins (ASEL0 from the LTC3887 is compatible with ASEL from the LTC3880), VOUT0_CONFIG, VOUT1_CONFIG, PHAS_CONFIG and FREQ_CONFIG.
- The LTC3880 has one address selection pin (ASEL), VOUT0_CONFIG, VOUT1_CONFIG, VTRIM0_CONFIG, VTRIM1_CONFIG, FREQ_CONFIG.
- Refer to the LTC3887 and LTC3880 data sheets for more detail on these configuration pins.

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ELECTRICAL CHARACTERISTICS

The electrical characteristics of the LTC3887 are the same as the LTC3880 with the following exceptions:

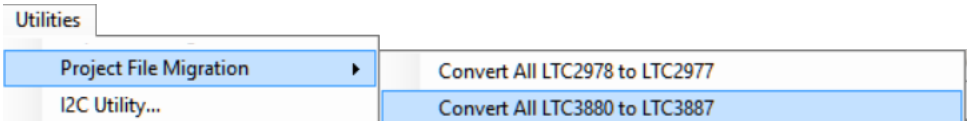
	LTC3880	LTC3887
T_{INIT} Startup Time	135ms	<70ms
V_{OUT} Maximum Voltage (V_{OUT0}/V_{OUT1})	4.0/5.4	5.5/5.5

CONFIGURATION FILE

The following PMBus commands are new or have changed in the LTC3887. An automatic conversion utility is provided in LTpowerPlay™ to simplify the transition from an LTC3880 configuration file to a functionally equivalent LTC3887 configuration file.

If you have an existing LTC3880 project file (.proj file), the simplest way to convert a LTC3880 configuration into a LTC3887 configuration is to use the built-in project file migration tool in LTpowerPlay. Follow this simple procedure to convert your project file:

- Launch LTpowerPlay
- Select “File > Open…” on the menu and browse to the project file containing one or more LTC3880 devices
- Select “Utilities > Project File Migration > Convert All LTC3880 to LTC3887” on the menu



After running the migration tool, all LTC3880s in your project file will be replaced with LTC3887 devices with equivalent configurations. For complete detail on how LTpowerPlay performs the migration at the register level, consult the “Writable Commands” section.

Read-Only Commands

The following read-only commands return different values on the LTC3880 and LTC3887. No configuration file changes are required, but if your software or firmware reads these registers and expects certain values, note that they have changed.

	LTC3880	LTC3887
MFR_SPECIAL_ID (0xE7)	0x040x	0x470x
PMBUS_REVISION (0x98)	0x11	0x22
MFR_MODEL (0x9A)	LTC3880	LTC3887

CONFIGURATION FILE

Writable Commands

A simple procedure exists to migrate an existing LTC3880 configuration for use in a LTC3887 device. The LTpowerPlay project file migration tool uses this procedure to automatically migrate your project file. The conversion details are provided below for those writing software/firmware and those wanting complete details on the migration process. Functions that require attention are listed in the table below, with the LTC3880 register and bit-field location shown in the second column, and the corresponding LTC3887 register and bit-field locations in the third column with the recommended action in the fourth column:

	LTC3880	LTC3887	PROCEDURE
Mask PLL_UNLOCK	MFR_CONFIG_ALL Bit 3	MASK_STATUS_MFR_SPECIFIC Bit 4	Move to new location.
Mask Pull GPIO Low (Paged)	MFR_CHAN_CONFIG Bit 1	MASK_STATUS_MFR_SPECIFIC Bit 0	Move to new location and disable in old location.
Set Channel 0 VRANGE LO/HI	MFR_PWM_CONFIG Bit 6	MFR_PWM_MODE Bit 1 (Page 0)	Move to new location.
Set Channel 1 VRANGE LO/HI	MFR_PWM_CONFIG Bit 5	MFR_PWM_MODE Bit 1 (Page 1)	Move to new location.
Set PWM to CCM (Paged)	MFR_PWM_MODE Bit 1 and 0 = 10	MFR_PWM_MODE Bit 0 = 1	Move to new location.
Set PWM to DCM (Paged)	MFR_PWM_MODE Bit 1 and 0 = 00 or 01	MFR_PWM_MODE Bit 0 = 0	Move to new location and Burst Mode operation set to CCM.*
Set SYNC Out to Off (for PolyPhase Sync Slaves)	FREQUENCY_SWITCH = 00 (External Clock)	MFR_CONFIG_ALL Bit 3 = 0	Change as specified.**
Set Frequency (for PolyPhase Sync Slaves)	FREQUENCY_SWITCH = 00 (External Clock)	FREQUENCY_SWITCH = Frequency of Rail Master	Change as specified.**
Disable CML Quick Read	Quick Read Always Disabled	MFR_CONFIG_ALL Bit 5 = 1	Set to 1/disabled for backward compatibility.
Enable 32ms Timeout	32ms Timeout Always Enabled	MFR_CONFIG_ALL Bit 3 = 0	Set to 0/enabled for backward compatibility.
Enable Channel 0 EA for Channel 1 PWM Control	Not Available	MFR_PWM_CONFG Bit 7 = 1	Set to 0/disabled. User must change manually if desired.***
PGOOD Thresholds	Used for ADC PGOOD	Uses OV/UV Thresholds.	PGOOD thresholds not used in LTC3887.
MFR_CHANNEL ADDRESS	Used to Communicate Directly with a Paged Command	Not Available, Use PAGE_PLUS if Atomic Commands Required	MFR_CHANNEL_ADDRESS is not used in the LTC3887.

* The LTC3880 in burst mode, MFR_PWM_MODE bits 1 and 0 set to 01, cannot be supported in the LTC3887. The closest option is DCM or MFR_PWM_MODE bit 0 set to 0.

** If and only if the project file has PolyPhase rails, LTpowerPlay infers frequency master of each rail as the chip whose FREQUENCY_SWITCH is programmed as non-zero. During migration, LTpowerPlay will set the slave chips' FREQUENCY_SWITCH register to match the master chip. In addition, the SYNC output will only be enabled on the master channel. For all non-PolyPhase rails or systems where LTpowerPlay cannot determine which chip is the frequency master (for instance, all FREQUENCY_SWITCH registers programmed to zero), the frequency commands will remain unchanged after the migration process.

*** This bit allows the differential sense amplifier from channel 0 to be the input to the channel 1 error amplifier. This bit may only be set if both channel 0 and channel 1 are part of the same PolyPhase rail and ITH0 and ITH1 are shorted. Because this bit may cause application problems if incorrectly set, it will be set to zero when projects are migrated. The LTC3880 does not support this command so no change in operation will occur.

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