NLAS3799B, NLAS3799BL

Dual DPDT Ultra-Low R$_{ON}$ Switch

The NLAS3799B is an ultra−low R$_{ON}$ dual DPDT and a 0.5 Ω R$_{ON}$ analog switch. This device is designed for low operating voltage, high current switching of speaker output and earpiece for cellphone applications. It can switch a balanced stereo output. The NLAS3799B can handle a balanced microphone/speaker/ring−tone generator in a monophone mode. The device contains a break−before−make (BBM) feature.

Features

- Single Supply Operation
    - 1.65 to 4.5 V V$_{CC}$
    - Function Directly from LiON Battery
- Maximum Breakdown Voltage: 5.5 V
- Low Static Power
- NLAS3799B Interfaces with 2.8 V Chipset
    NLAS3799BL Interfaces with 1.8 V Chipset
- These are Pb−Free Devices

Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone−Chip/Amplifier Switching
- Four Unbalanced (Single−Ended) Switches
- Stereo Balanced (Push−Pull) Switching
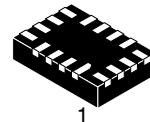
Important Information

- ESD Protection:
    - Human Body Model (HBM) > 8000 V
    - Machine Model (MM) > 400 V
- Continuous Current Rating Through each Switch ±300 mA
- Conforms to: JEDEC MO−220, Issue H, Variation VEED−6
- Package:
    - 1.8 x 2.6 x 0.75 mm WQFN−16 Pb−Free
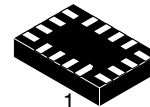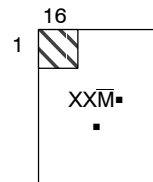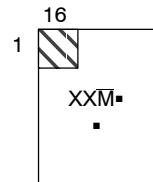   - 1.8 x 2.6 x 0.55 mm UQFN−16 Pb−Free

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS
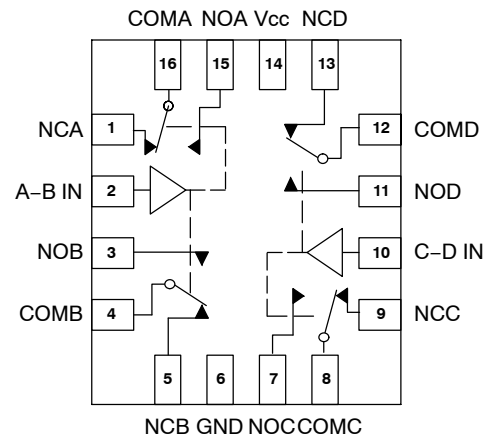

WQFN−16
CASE 488AP

UQFN−16
CASE 488AU

XX = Specific Device Code
- AK = NLAS3799BMNR2G
- AL = NLAS3799BLMNR2G
- AX = NLAS3799BMUR2G

$\overline{M}$ = Date Code/Assembly Location

▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

Figure 1. Input Equivalent Circuit
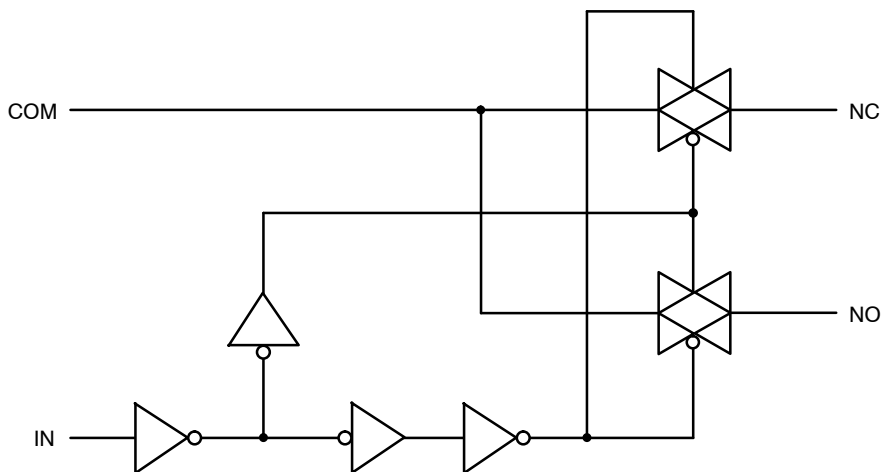
PIN DESCRIPTION

QFN PIN #	Symbol	Name and Function
1, 3, 5, 7, 9, 11, 13, 15	NO A–D, NC A–D	Independent Channels
2, 10	A–B IN, C–D IN	Controls
4, 8, 12, 16	COM A–D	Common Channels
6	GND	Ground (V)
14	V$_{CC}$	Positive Supply Voltage

TRUTH TABLE

IN	NO	NC
H	ON	OFF*
L	OFF*	ON

*High impedance.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	−0.5 to +5.5	V
V_{IS}	Analog Input Voltage (V_{NO}, V_{NC}, or V_{COM})	$-0.5 \leq V_{IS} \leq V_{CC} + 0.5$	V
V_{IN}	Digital Select Input Voltage	$-0.5 \leq V_{IN} \leq +V_{CC}$	V
I_{anl1}	Continuous DC Current from COM to NC/NO	±300	mA
$I_{anl-pk1}$	Peak Current from COM to NC/NO, 10 Duty Cycle (Note 1)	±500	mA
I_{clmp}	Continuous DC Current into COM/NO/NC with Respect to V_{CC} or GND	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Defined as 10% ON, 90% OFF Duty Cycle.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.65	4.5	V
V_{IN}	Digital Select Input Voltage		GND	V_{CC}	V
V_{IS}	Analog Input Voltage (NC, NO, COM)		GND	V_{CC}	V
T_A	Operating Temperature Range		−40	+85	°C
t_r, t_f	Input Rise or Fall Time, IN	V_{CC} = 1.6 V – 2.7 V V_{CC} = 3.0 V – 4.5 V		20 10	ns/V

NLAS3799B DC CHARACTERISTICS − DIGITAL SECTION (Voltages Referenced to GND)

Symbol	Parameter	Condition	V$_{CC}$	Guaranteed Limit		Unit
				25°C	−40°C to +85°C	
V$_{IH}$	Minimum High−Level Input Voltage, Select Inputs		3.0 4.3	1.4 2.0	1.4 2.0	V
V$_{IL}$	Maximum Low−Level Input Voltage, Select Inputs		3.0 4.3	0.5 0.8	0.5 0.8	V
I$_{IN}$	Maximum Input Leakage Current, Select Inputs	V$_{IN}$ = V$_{CC}$ or GND	4.3	±0.1	±1.0	µA
I$_{OFF}$	Power Off Leakage Current	V$_{IN}$ = 4.5 V or GND	0	±0.5	±2.0	µA
I$_{CC}$	Maximum Quiescent Supply Current (Note 2)	Select and V$_{IS}$ = V$_{CC}$ or GND	1.65 to 4.5	±1.0	±2.0	µA

2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

NLAS3799B DC ELECTRICAL CHARACTERISTICS − ANALOG SECTION

Symbol	Parameter	Condition	V$_{CC}$	Guaranteed Maximum Limit				Unit
				25°C		−40°C to +85°C		
				Min	Max	Min	Max	
R$_{ON}$	NC/NO On−Resistance (Note 3)	V$_{IN}$ = V$_{IL}$ or V$_{IN}$ = V$_{IH}$ V$_{IS}$ = GND to V$_{CC}$ I$_{IN}$I = 100 mA	3.0 4.3		0.5 0.4		0.6 0.5	Ω
R$_{FLAT}$	NC/NO On−Resistance Flatness (Notes 3 and 4)	I$_{COM}$ = 100 mA V$_{IS}$ = 0 to V$_{CC}$	3.0 4.3		0.15 0.15		0.15 0.15	Ω
ΔR$_{ON}$	On−Resistance Match Between Channels (Notes 3 and 5)	V$_{IS}$ = 1.5 V; I$_{COM}$ = 100 mA V$_{IS}$ = 2.2 V; I$_{COM}$ = 100 mA	3.0 4.3		0.05 0.05		0.05 0.05	Ω
I$_{NC(OFF)}$ I$_{NO(OFF)}$	NC or NO Off Leakage Current (Note 3)	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ V$_{NO}$ or V$_{NC}$ = 0.3 V V$_{COM}$ = 4.0 V	4.3	−10	10	−100	100	nA
I$_{COM(ON)}$	COM ON Leakage Current (Note 3)	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ V$_{NO}$ 0.3 V or 4.0 V with V$_{NC}$ floating or V$_{NC}$ 0.3 V or 4.0 V with V$_{NO}$ floating V$_{COM}$ = 0.3 V or 4.0 V	4.3	−10	10	−100	100	nA

3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
4. Flatness is defined as the difference between the maximum and minimum value of On−resistance as measured over the specified analog signal ranges.
5. ΔR$_{ON}$ = R$_{ON(MAX)}$ − R$_{ON(MIN)}$ between NCn or NOn.

NLAS3799BL DC CHARACTERISTICS – DIGITAL SECTION (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit		Unit
				25°C	−40 to +85°C	
V_{IH}	Minimum High−Level Input Voltage, Select Inputs		3.0 4.3	1.3 1.6	1.3 1.6	V
V_{IL}	Maximum Low−Level Input Voltage, Select Inputs		3.0 4.3	0.5 0.6	0.5 0.6	V
I_{IN}	Maximum Input Leakage Current, Select Inputs	$V_{IN} = V_{CC}$ or GND	4.3	±0.1	±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 4.5 V or GND	0	±0.5	±2.0	μA
I_{CC}	Maximum Quiescent Supply Current (Note 6)	Select and $V_{IS} = V_{CC}$ or GND	1.65 to 4.3	±40	±45	μA

6. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

NLAS3799BL DC ELECTRICAL CHARACTERISTICS – ANALOG SECTION

Symbol	Parameter	Condition	V_{CC}	Guaranteed Maximum Limit				Unit
				25°C		−40°C to +85°C		
				Min	Max	Min	Max	
R_{ON}	NC/NO On−Resistance (Note 7)	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ V_{IS} = GND to V_{CC} I_{IN}I = 100 mA	3.0 4.3		0.5 0.4		0.6 0.5	Ω
R_{FLAT}	NC/NO On−Resistance Flatness (Notes 7 and 8)	I_{COM} = 100 mA V_{IS} = 0 to V_{CC}	3.0 4.3		0.15 0.15		0.15 0.15	Ω
ΔR_{ON}	On−Resistance Match Between Channels (Notes 7 and 9)	V_{IS} = 1.5 V; I_{COM} = 100 mA V_{IS} = 2.2 V; I_{COM} = 100 mA	3.0 4.3		0.05 0.05		0.05 0.05	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	NC or NO Off Leakage Current (Note 7)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} or V_{NC} = 0.3 V V_{COM} = 4.0 V	4.3	−10	10	−100	100	nA
$I_{COM(ON)}$	COM ON Leakage Current (Note 7)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} 0.3 V or 4.0 V with V_{NC} floating or V_{NC} 0.3 V or 4.0 V with V_{NO} floating V_{COM} = 0.3 V or 4.0 V	4.3	−10	10	−100	100	nA

7. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
8. Flatness is defined as the difference between the maximum and minimum value of On−resistance as measured over the specified analog signal ranges.
9. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ between NC1 and NC2 or between NO1 and NO2.

NLAS3799B/NLAS3799BL AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	V_{IS} (V)	Guaranteed Maximum Limit					Unit
					25°C			−40°C to +85°C		
					Min	Typ*	Max	Min	Max	
t_{ON}	Turn−On Time	$R_L = 50\ \Omega$, $C_L = 35$ pF (Figures 3 and 4)	2.3 – 4.3	1.5			50		60	ns
t_{OFF}	Turn−Off Time	$R_L = 50\ \Omega$, $C_L = 35$ pF (Figures 3 and 4)	2.3 – 4.3	1.5			30		40	ns
t_{BBM}	Minimum Break−Before−Make Time	$V_{IS} = 3.0$ $R_L = 50\ \Omega$, $C_L = 35$ pF (Figure 2)	3.0	1.5	2	15				ns

		Typical @ 25, V_{CC} = 3.6 V	
C_{IN}	Control Pin Input Capacitance	3.0	pF
C_{SN}	SN Port Capacitance	72	pF
C_D	D Port Capacitance When Switch is Enabled	220	pF

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V_{CC} (V)	25°C Typical	Unit
BW	Maximum On−Channel −3 dB Bandwidth or Minimum Frequency Response (Figure 9)	V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	19	MHz
V_{ONL}	Maximum Feed−through On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	−0.06	dB
V_{ISO}	Off−Channel Isolation	f = 100 kHz; $V_{IS} = 1$ V RMS; $C_L = 5.0$ pF V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	−69	dB
Q	Charge Injection Select Input to Common I/O (Figure 8)	$V_{IN} = V_{CC}$ to GND, $R_{IS} = 0\ \Omega$, $C_L = 1.0$ nF $Q = C_L \times \Delta V_{OUT}$ (Figure 6)	1.65 – 4.5	51	pC
THD	Total Harmonic Distortion THD + Noise (Figure 7)	$F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600\ \Omega$, $C_L = 50$ pF $V_{IS} = 2\ V_{PP}$	4.3	0.042	%
VCT	Channel−to−Channel Crosstalk (Figure 10)	f = 100 kHz; $V_{IS} = 1.0$ V RMS, $C_L = 5.0$ pF, $R_L = 50\ \Omega$ V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	−90	dB

10. Off−Channel Isolation = $20\log10\ (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.
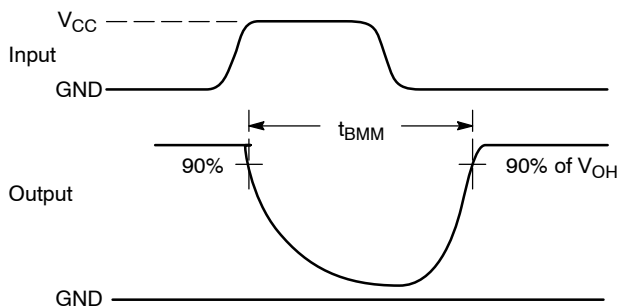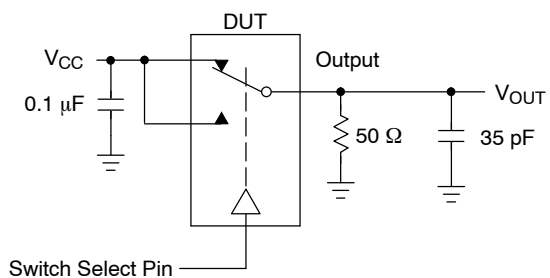
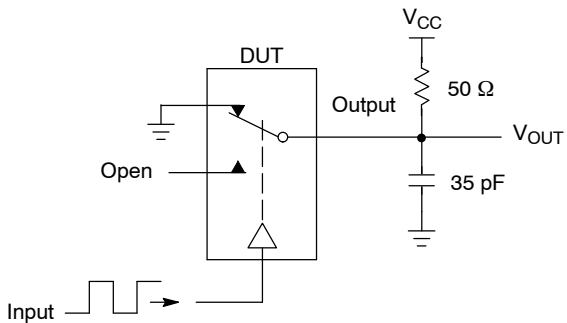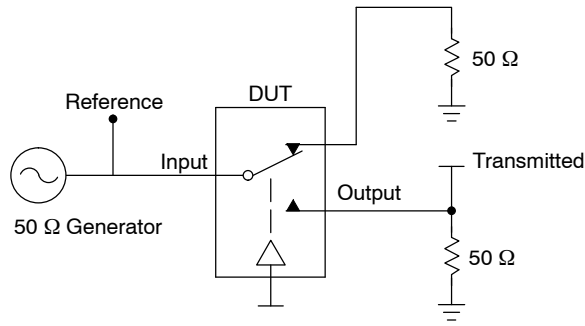**Figure 2. t$_{BBM}$ (Time Break−Before−Make)**
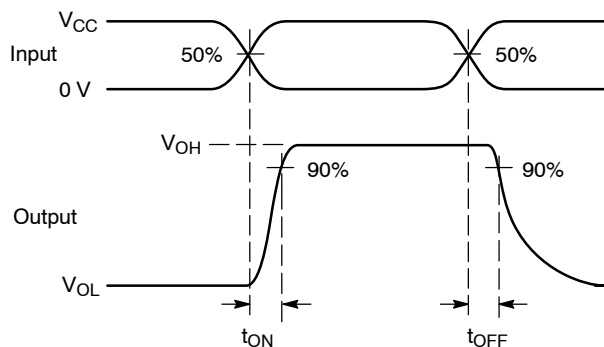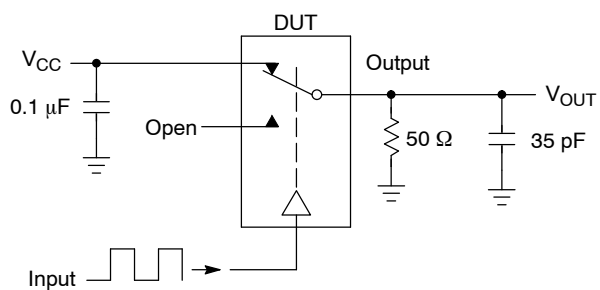
Figure 3. t$_{ON}$/t$_{OFF}$
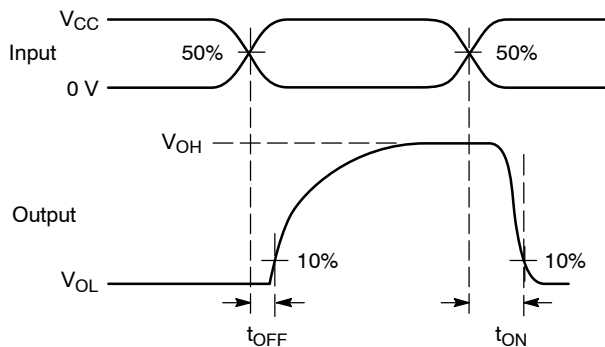
Figure 4. t$_{ON}$/t$_{OFF}$

Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = $20 \, Log \left(\dfrac{V_{OUT}}{V_{IN}} \right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = $20 \, Log \left(\dfrac{V_{OUT}}{V_{IN}} \right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk
(On Channel to Off Channel)/V_{ONL}
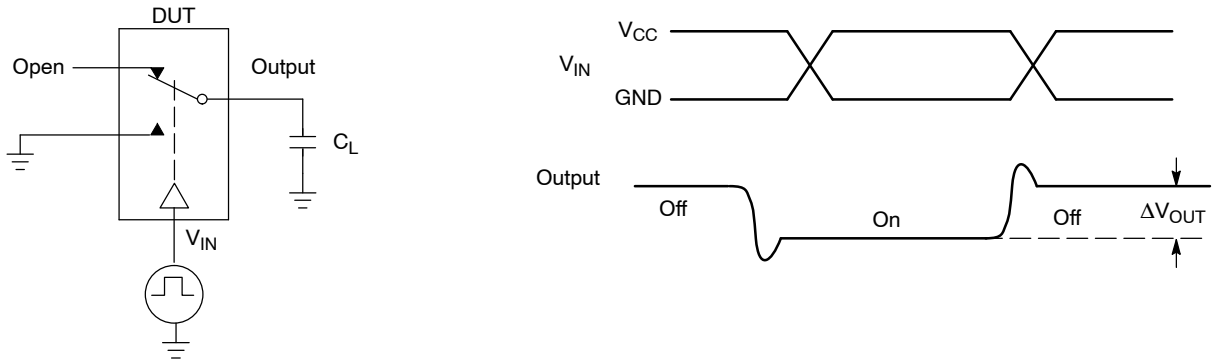
Figure 6. Charge Injection: (Q)
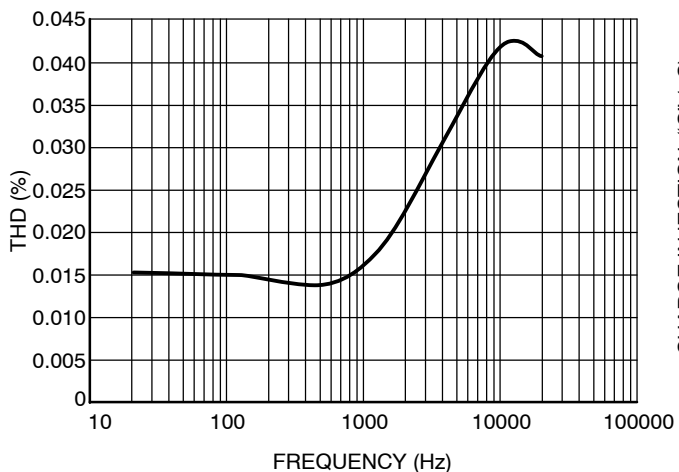
Figure 7. Total Harmonic Distortion vs. Frequency
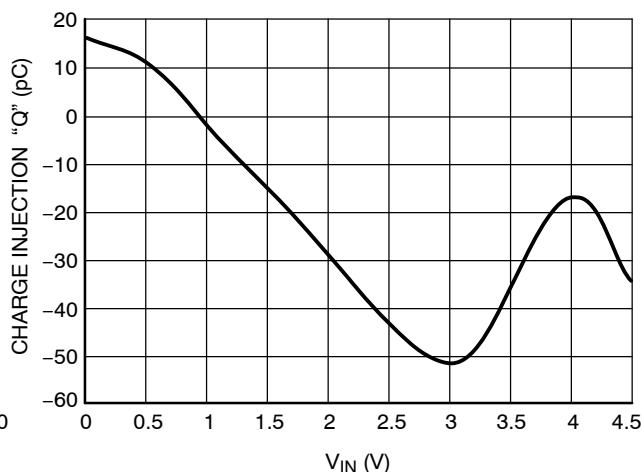
Figure 8. Charge Injection @ 0 V < V$_{CC}$ < 4.5 V
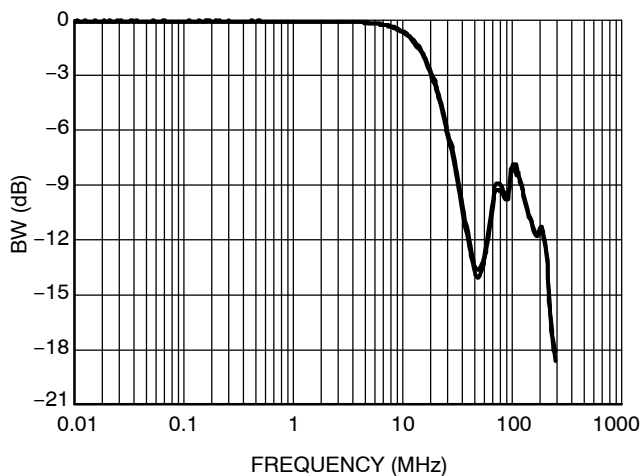
Figure 9. Bandwidth vs. Frequency
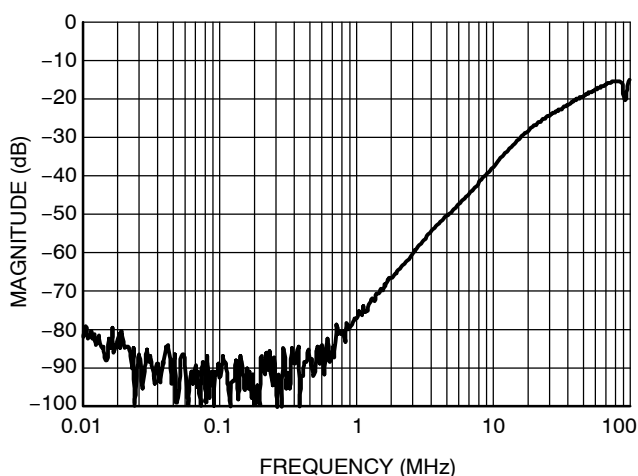
Figure 10. Cross−Talk vs. Frequency
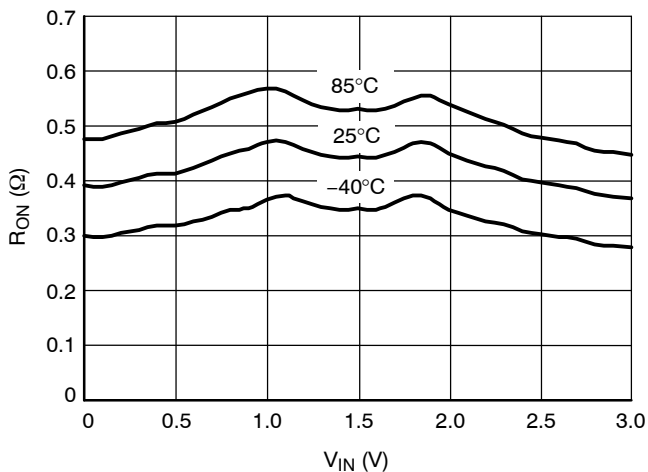
Figure 11. R$_{ON}$ vs. V$_{IN}$ vs. Temperature @ V$_{CC}$ = 3.0 V
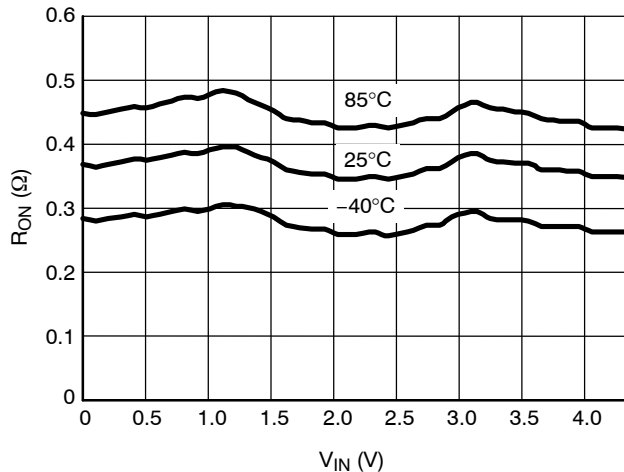
Figure 12. R$_{ON}$ vs. V$_{IN}$ vs. Temperature @ V$_{CC}$ = 4.3 V

DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape & Reel Size†
NLAS3799BMNR2G	WQFN–16 (Pb–Free)	3000 / Tape & Reel
NLAS3799BLMNR2G	WQFN–16 (Pb–Free)	3000 / Tape & Reel
NLAS3799BMUR2G	UQFN–16 (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WQFN16, 1.8x2.6, 0.4P
CASE 488AP−01
ISSUE B
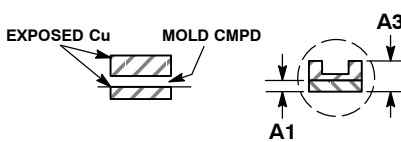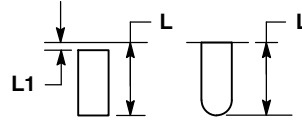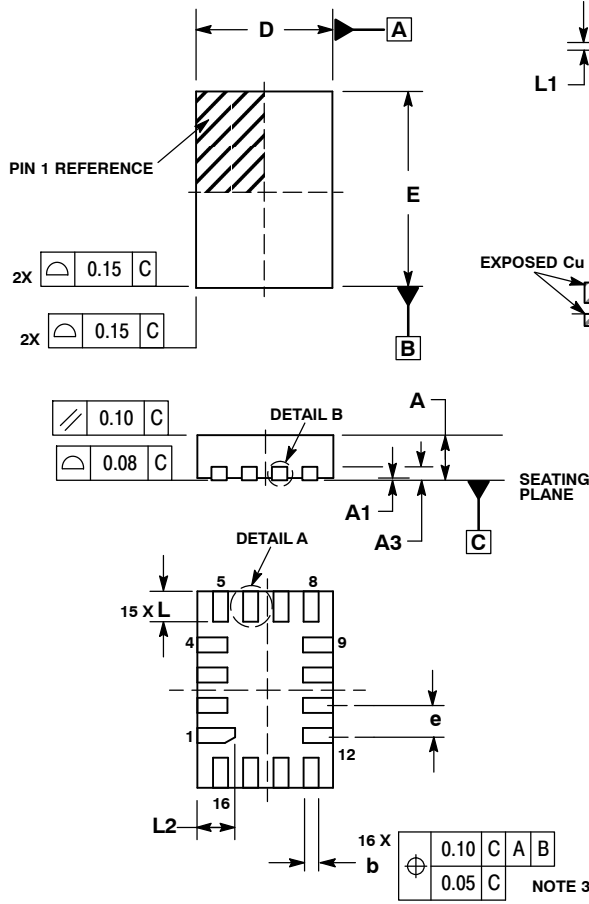
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

DETAIL B
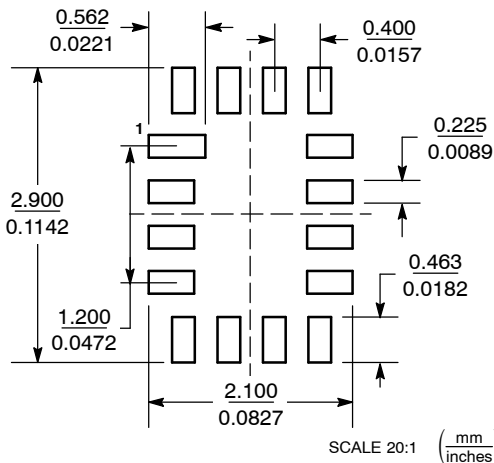ALTERNATE
CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L2	0.40	0.60

MOUNTING FOOTPRINT*
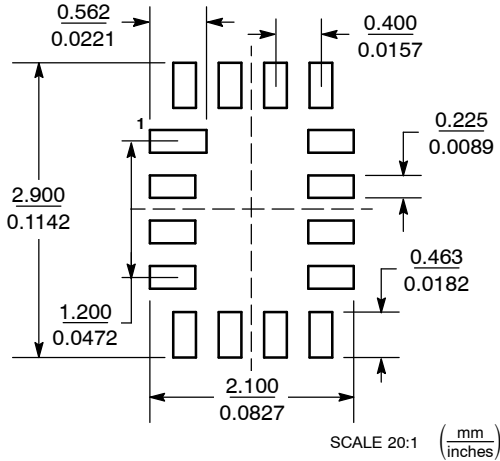
SCALE 20:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLAS3799B, NLAS3799BL

PACKAGE DIMENSIONS

UQFN16, 1.8x2.6, 0.4P
CASE 488AU−01
ISSUE A
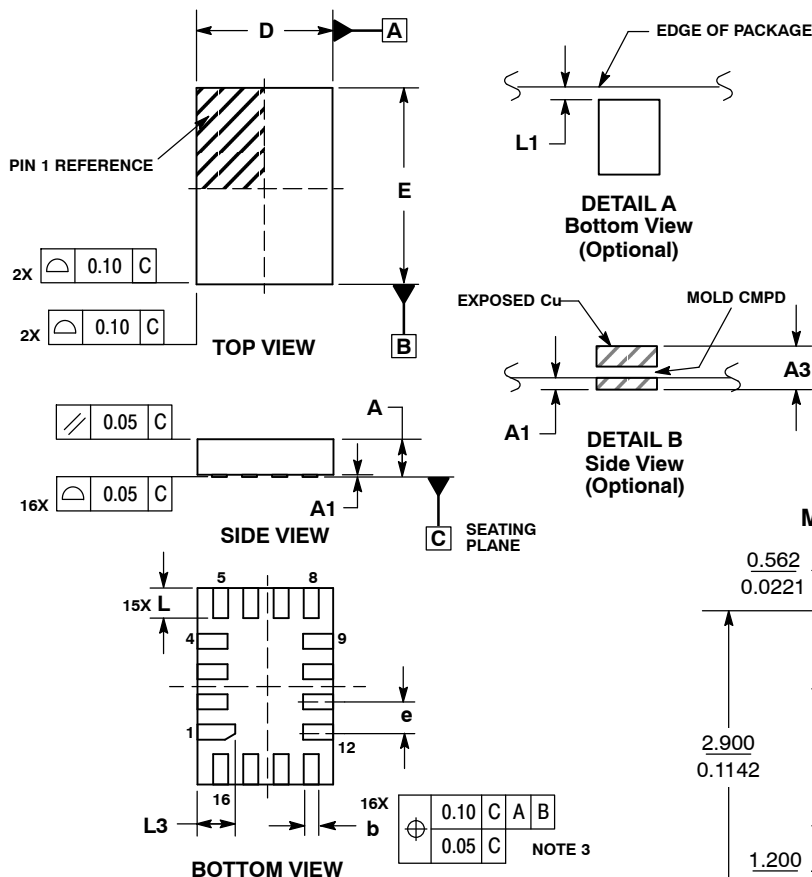
PIN 1 REFERENCE

2X ⌀ 0.10 C

2X ⌀ 0.10 C

TOP VIEW

D

E

A

B

EDGE OF PACKAGE

L1

DETAIL A
Bottom View
(Optional)

EXPOSED Cu   MOLD CMPD

A3

A1

DETAIL B
Side View
(Optional)

0.05 C

16X ⌀ 0.05 C

SIDE VIEW

A

A1

C **SEATING PLANE**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

15X L

5   8

4   9

e

1   12

L3   16   16X b

⊕ | 0.10 | C A B
    | 0.05 | C   NOTE 3

BOTTOM VIEW

MOUNTING FOOTPRINT*

$\frac{0.562}{0.0221}$

$\frac{0.400}{0.0157}$

$\frac{0.225}{0.0089}$

$\frac{2.900}{0.1142}$

$\frac{0.463}{0.0182}$

$\frac{1.200}{0.0472}$

$\frac{2.100}{0.0827}$

SCALE 20:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLAS3799B/D