PE22100

Document Category: Product Specification

Transformer Driver for Isolated Power Supplies, 2 MHz

Features

- Push pull driver for small transformers
- Operates off a 3.0V or 5V supply
- Adjustable switching frequency up to 2 MHz
- Current limit protection
- Over-temperature protection
- Packaging – 2 × 2 × 0.5 mm QFN

Applications

- Isolated interface power supply
- Isolated data acquisition
- Industrial automation and instrumentation
- Isolated gate drivers
- Medical equipment

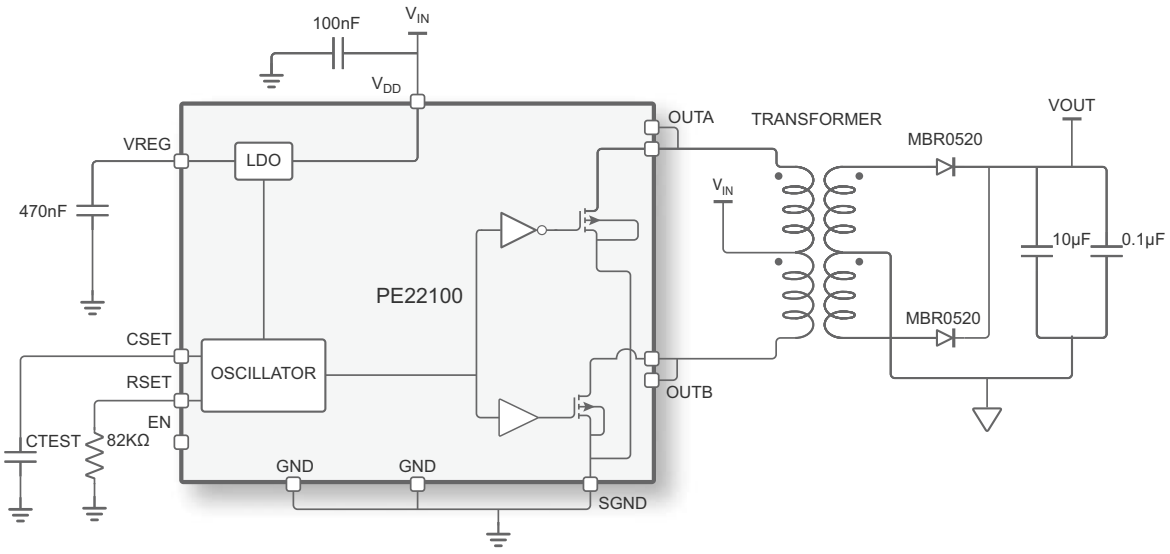
Product Description

The PE22100 is a push pull driver for driving small transformers for isolated power supply applications. The PE22100 drives the primary of a center-tapped transformer, such as the 782100 family from Murata, from a 3.0V or a 5V supply to deliver an isolated power supply.

The device consists of an on-chip oscillator whose frequency is set by an external capacitor. The oscillator output is divided by two in frequency to create anti-phase clock signals that drive two power switches. The device also contains an internal current limit and thermal cutout. The PE22100 is available in a 2 × 2 × 0.5 mm QFN package and is specified for operation from –40 °C to +125 °C.

The PE22100 is manufactured on Peregrine's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1 • *PE22100 Functional Diagram*



Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 3**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 1 • *Absolute Maximum Ratings for PE22100*

Parameter/Condition	Min	Max	Unit
V_{DD}		7	V
Voltage on OUTA or OUTB		15	V
Switch current		350	mA
Enable pin voltage		V_{REG} +0.3	V

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 2**.

Table 2 • *ESD Tolerance*

Parameter/Condition	Max	Unit
Human Body model all pins/tested to JEDEC JS–001	1	kV

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Recommended Operating Conditions

Table 3 lists the recommending operating conditions for the PE22100. Devices should not be operated outside the operating conditions listed below.

Table 3 • *Recommended Operating Conditions for PE22100*

Parameter	Min	Typ	Max	Unit
Positive supply voltage, V_{DD}	3.0	5.0	5.5	V
Positive supply current, I_{DD}			10.6	mA
Switch voltage on OUTA and OUTB			11	V
Transient on OUTA or OUTB(*)			15	V
Note: * Max width 20 ns, max duty cycle 1:100.				

Electrical Specifications

Table 4 provides the PE22100 key electrical specifications at 25 °C, unless otherwise specified.

Table 4 • *PE22100 Electrical Specifications*

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		100 kHz		2 MHz	As shown
Minimum switching frequency	C_{SET} =100pF	170	235	275	KHz
Maximum switching frequency	C_{SET} =8.2pF	2240	2290	2504	KHz
Output switch resistance	V_{DD}=5V T=–40°C to +105°C ambient, measured OUTA to GND, OUTB to GND		1	1.3	Ω
Oscillating frequency accuracy	Excluding external component variation	–15		+15	%
Over temperature assert		+126		+162	°C
Over temperature hysteresis			3.4		°C
Over current protection assert		540			mA
Over current protection current	With 2V across OUTA, OUTB to GND	280			mA
Undervoltage-lockout (UVLO) assert				2.5	V
UVLO threshold			2.45		V
UVLO hysteresis			20		mV
Output rise and fall time	Cload<50pF			5.5	ns
Internal regulated voltage at V_{REG}	Internal regulated voltage at V_{REG}		2.6		V
Idd current shutdown	V_{sw}=V_{DD}=5V, both pulled high OUTA and OUTB		2.2	2.9	mA
Enable pin high	Input open circuit(*)	2.0	2.5		V
Enable pin low	Input pulled low(*)			0.7	V
Enable pin current	Enable pin voltage = 0V		8.3	10.0	µA
Oscillator capacitor charge/discharge current	R_{SET}=82kohms	32		45	µA

Note: * The enable pin is internally pulled up to the internal regulator. Voltages higher than VREG can damage the part.

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 5 • *Thermal Data for PE22100*

Parameter	Max	Unit
Tjc	20	°C/W
Maximum junction temperature(1)	125	°C
Soldering temperature(2)	245	°C
Soldering temperature(3)	260	°C
Ψ_{JT}	1.6	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	80.8	°C/W
Ψ_{JB}, junction-to-ambient thermal resistance	56.0	°C/W

Notes:
1) Simulated / Measured at max TA & max Power dissipation.
2) Reflow soldering J-STD-020D) 3 reflows.
3) Reflow soldering - 3 reflows

Typical Performance Data

Figure 2–Figure 4 show the typical performance data at V_{IN} = 3.3V, V_{OUT} = 3.3V, and use Murata transformer 782100/33VC.

Figure 2 • *Efficiency and Output Voltage, C_{SET} = 47 pF*

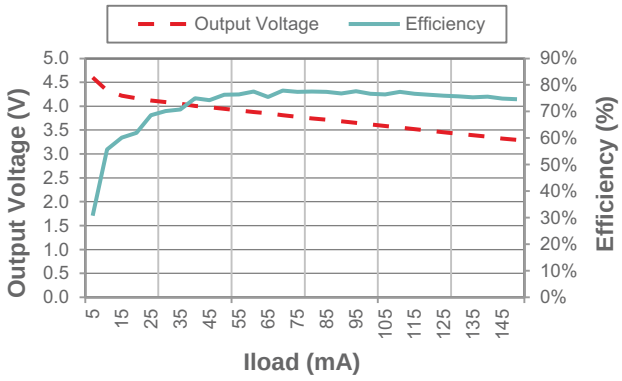


Figure 3 • *Efficiency and Output Voltage, C_{SET} = 100 pF*

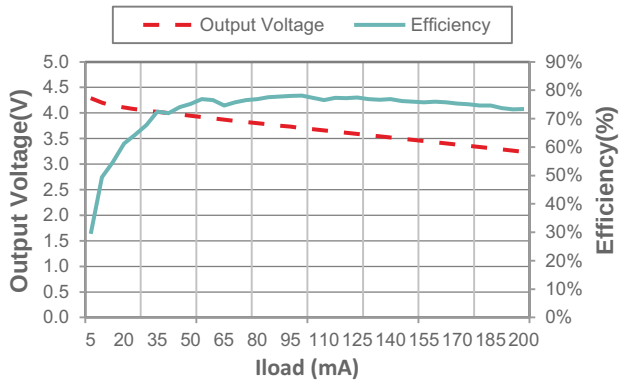


Figure 4 • *Efficiency and Output Voltage, C_{SET} = 220 pF*

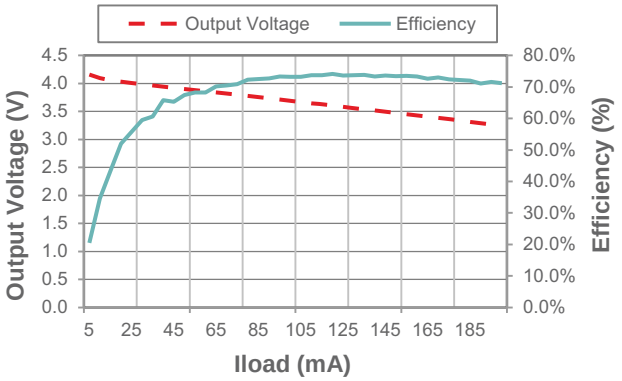


Figure 5–Figure 6 show the typical performance data at V_{IN} = 3.3V, V_{OUT} = 5V, and use transformer 782100/35JVC.

Figure 5 • *Efficiency and Output Voltage, C_{SET} = 47 pF*

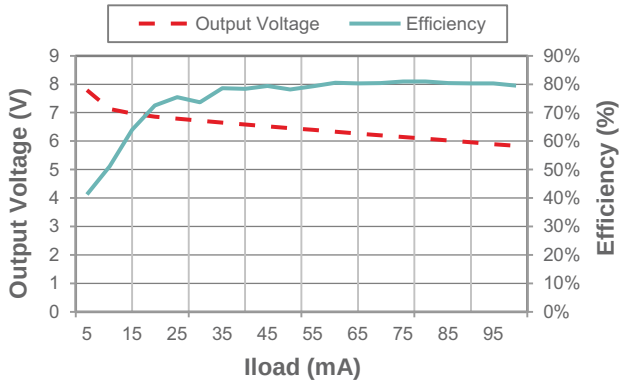


Figure 7 • *Efficiency and Output Voltage, C_{SET} = 100 pF*

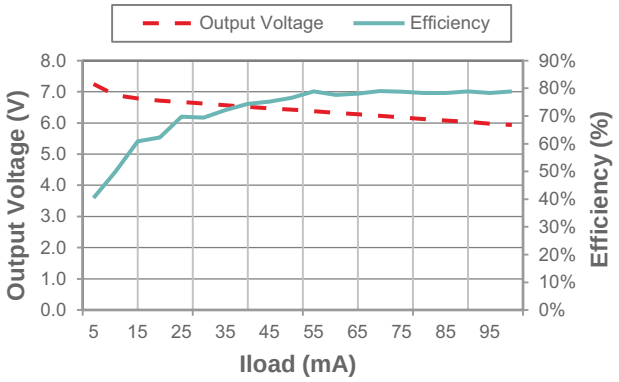


Figure 6 • *Efficiency and Output Voltage, C_{SET} = 220 pF*

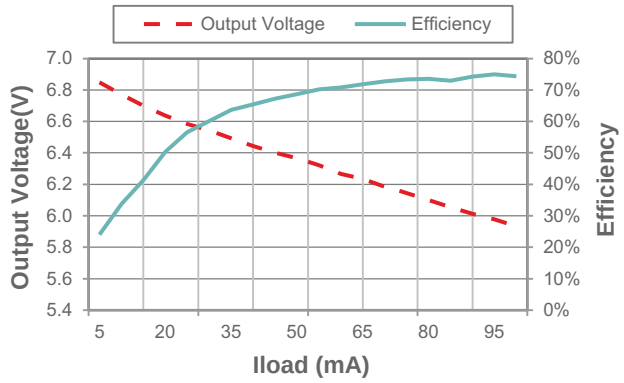


Figure 8–Figure 9 show the typical performance data at V_{IN} = 5V, V_{OUT} = 5V, and use transformer 782100/55JVC.

Figure 8 • *Efficiency and Output Voltage, C_{SET} = 47 pF*

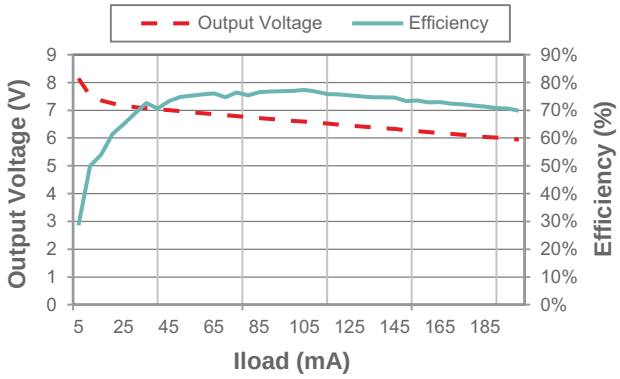


Figure 10 • *Efficiency and Output Voltage, C_{SET} = 100 pF*

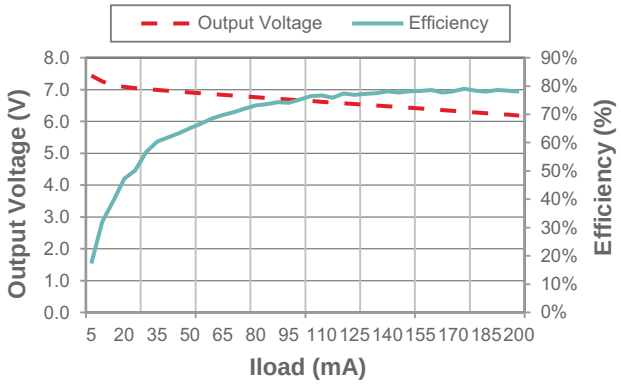


Figure 9 • *Efficiency and Output Voltage, C_{SET} = 220 pF*

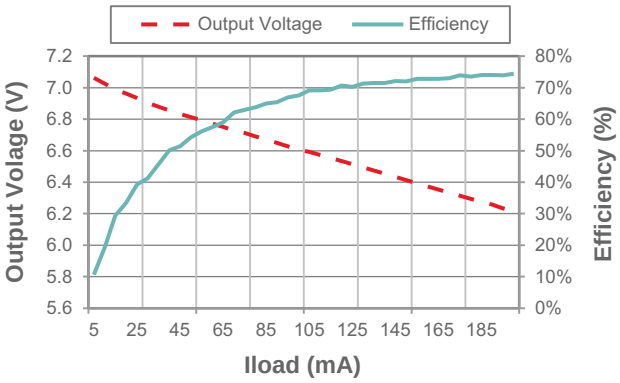


Figure 11–Figure 13 show the typical performance data at V_{IN} = 5V, V_{OUT} = 3.3V, and use transformer 7821053VC.

Figure 11 • *Efficiency and Output Voltage, C_{SET} = 47 pF*

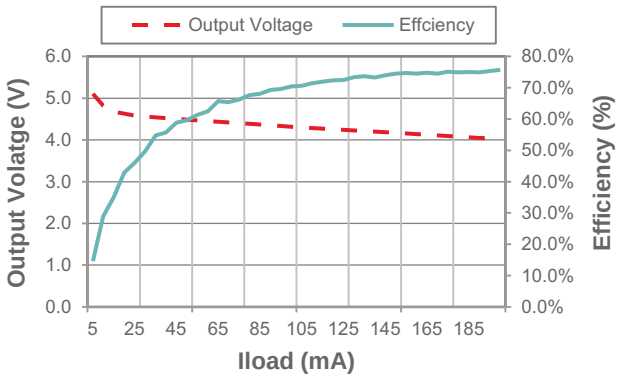


Figure 12 • *Efficiency and Output Voltage, C_{SET} = 100 pF*

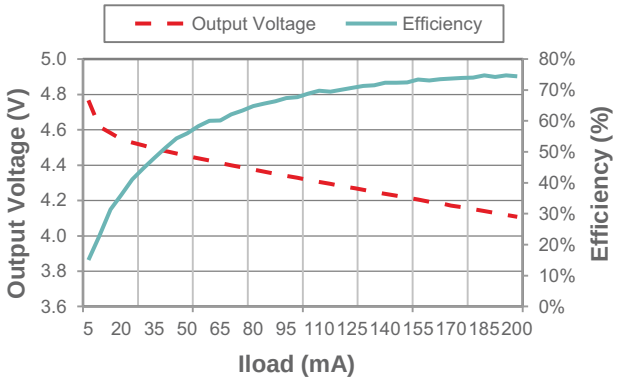
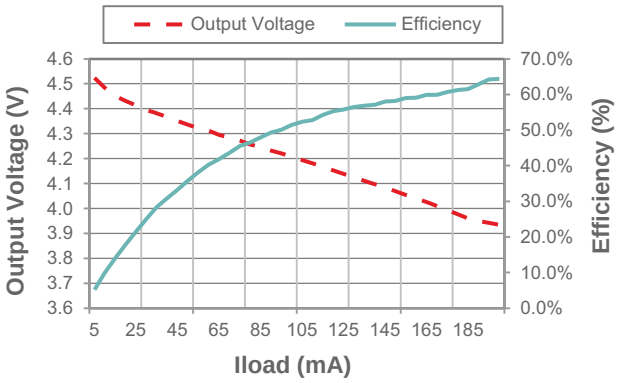


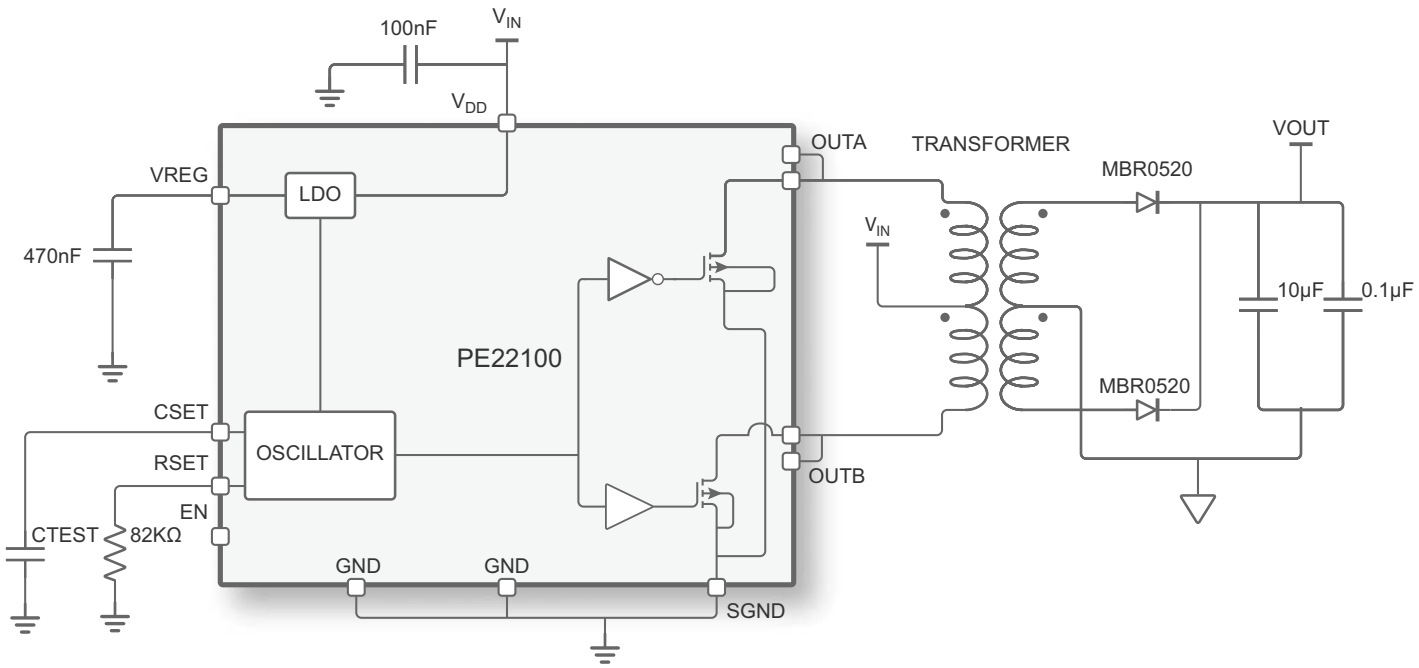
Figure 13 • *Efficiency and Output Voltage, C_{SET} = 220 pF*



Test Circuit 1

The test circuit is used for taking efficiency and output voltage measurements in **Figure 2–Figure 13**. All data is taken from the input and output voltage points and includes the diode drop.

Figure 14 • *Test Circuit 1*(*)

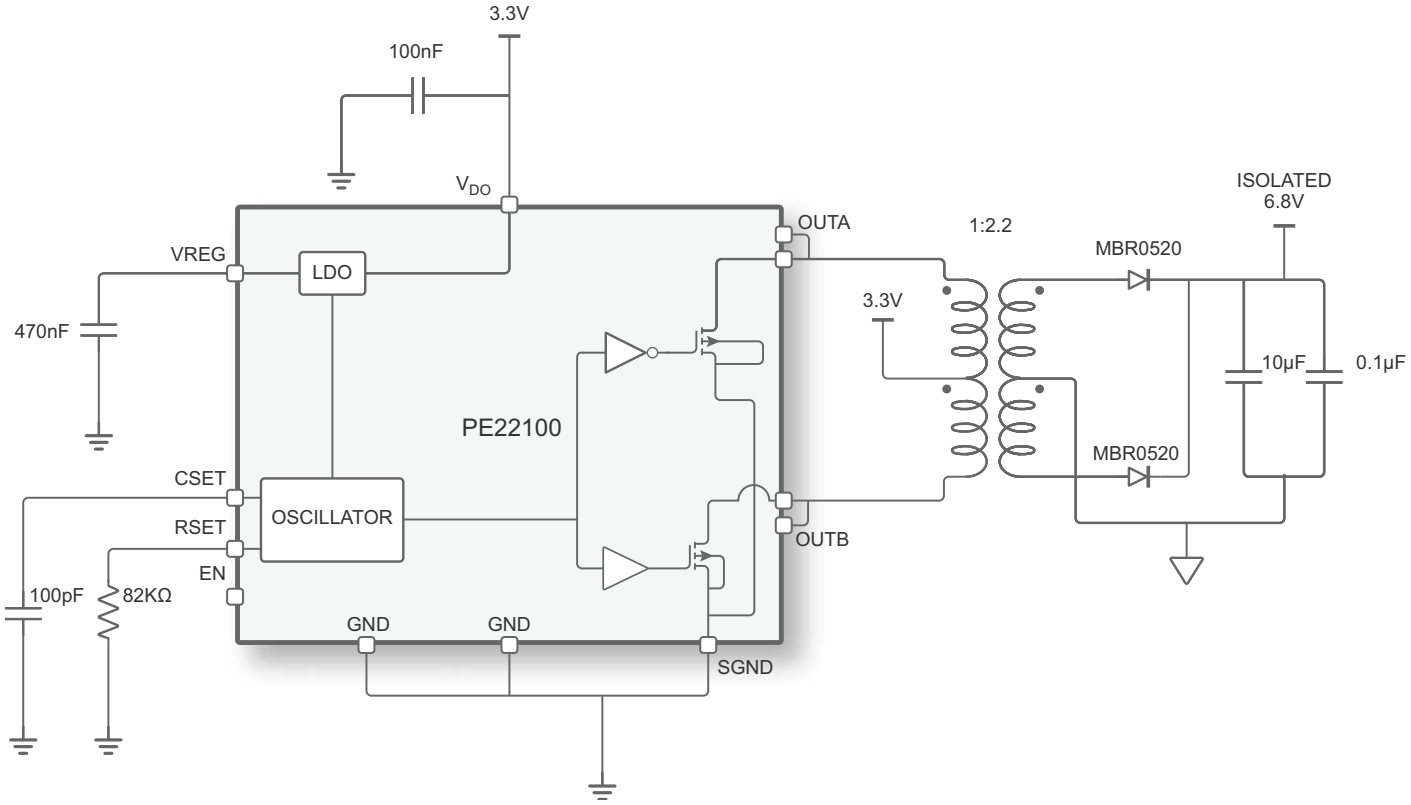


Note: * Efficiency measurements are made for the full circuit and include losses from the Schottky diodes.

Typical Operating Circuit

The circuit in **Figure 15** shows a typical configuration of PE22100 to generate an isolated power supply.

Figure 15 • *Typical Operating Circuit*



Theory of Operation

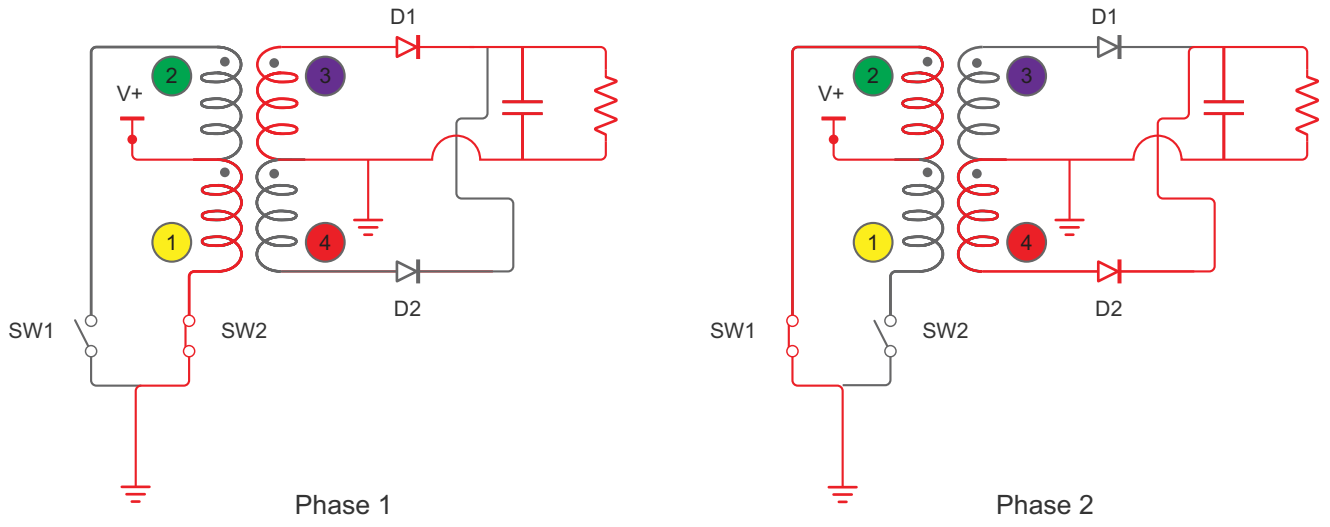
The PE22100 is a push pull transformer driver designed for use in isolated DC-DC applications. The device includes an oscillator that drives two internal FETs via an internal gate drive circuit. The gate drive circuitry provides two complimentary output signals that turn the output transistors on and off.

The oscillator's output frequency is set by RSET, and then internally divided by two to drive the transistors with a 50/50 duty cycle.

Operation of a Push Pull Converter

Push pull converters use center tapped transformers to transfer power from the primary to the secondary. The PE22100 contains two FETs to ground, represented by SW1 and SW2, that operate in two phases (see **Figure 16**).

Figure 16 • *PE22100 Operating Modes*(*)



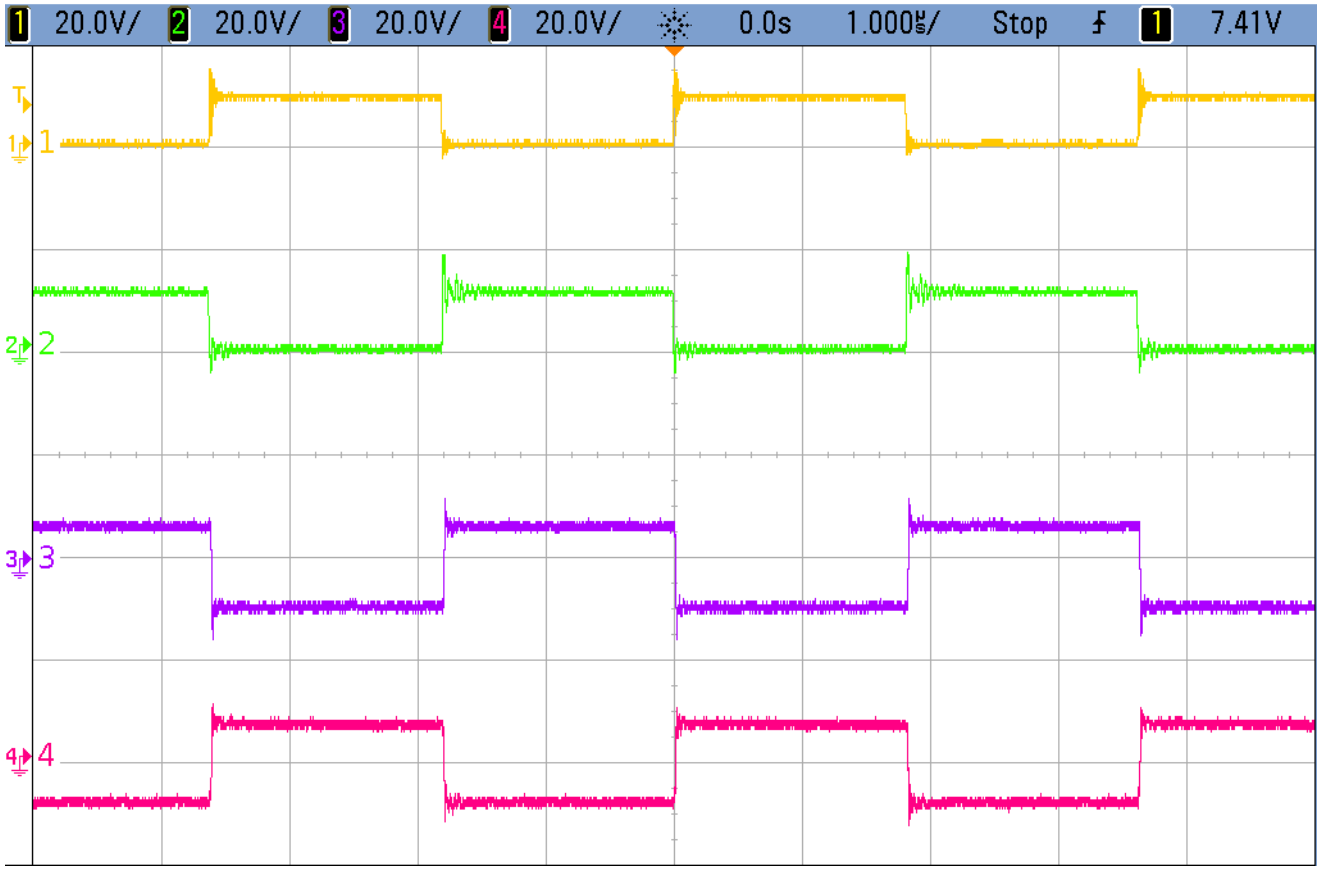
Note: * The numbers and colors in **Figure 16** correspond to the scope plot in **Figure 17**.

In Phase 1, the primary is energized (1) via SW2 being switched "ON" to ground. Then, during Phase 2, when SW2 is switched "OFF", the stored energy transfers (4) to the output capacitor via D2.

In Phase 2, the primary is energized (2) via SW1 being switched "ON" to ground. Then, during Phase 1, when SW1 is switched "OFF", the stored energy transfers (3) to the output capacitor via D1.

Cycling between Phases 1 and 2 continuously ensures that current is supplied to the output capacitor.

Figure 17 • *Switching Waveforms of the Transformer Colors*(*)



Note: * The switching waveforms of transformer colors correspond to the test points in **Figure 15** (RSET= 82 kΩ and CSET = 47 pF).

Recommended Isolation Transformers

The transformer used with the PE22100 must have sufficient energy handling capability (i.e., Et constant) to prevent saturation. The transformers in **Table 6** have been tested to work with the PE22100.

Table 6 • *Compatible Transformers*

Application	Murata Part Number	Isolation	VxT V/µS
3.3–3.3V	782100/33VC	4 kV	13
3.3–5V	782100/35JVC	4 kV	30
5–5V	782100/55JVC	4 kV	37
5–3.3V	782100/53VC	4 kV	13

Current Limit and Over-Temperature Detection

The PE22100 contains a built-in current limit feature. If the current in either OUTA or OUTB to GND exceeds 600 mA, both outputs will enter over current mode. In over current mode, the outputs continue to switch on and off in antiphase, but at a reduced over-current mode of 320 mA.

Both outputs maintain this current limit for 4096 clock cycles, as set by CSET, or until the over-temperature detection threshold is crossed, whichever occurs first.

After 4096 clock cycles, the current limit is checked again.

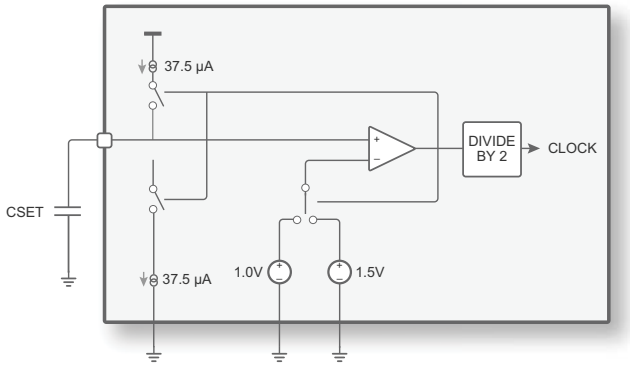
- If the current limit is below the threshold, the PE22100 exits current limit mode.
- If the current limit is above the current limit threshold, the PE22100 enters current limit mode for another 4096 clock cycles.

If the die temperature exceeds +140 °C, the internal FETs switch off, forming an open circuit at OUTA and OUTB. The temperature detector has an approximate hysteresis of +3.4 °C. As the temperature falls below the threshold, OUTA and OUTB resume normal operation.

Setting the Oscillator Frequency

The oscillator is based on a relaxation oscillator charging an external capacitor CSET. The charge and discharge current are set by the RSET value (see **Figure 18**). This forms an oscillator that charges and discharges capacitor CSET between 1.0V and 1.5V.

Figure 18 • *Internal Oscillator Structure*



To calculate the oscillator frequency at CSET:

$$\text{Frequency} = \frac{37.5\ \mu A}{CSET}$$

For example, the oscillator frequency at CSET for an external capacitor of 100 pF will be:

$$\text{Frequency} = \frac{37.5\ \mu a}{CSET} = \frac{37.5 \times 10^{-6}}{100 \times 10^{-12}} = 375\ \text{kHz}$$

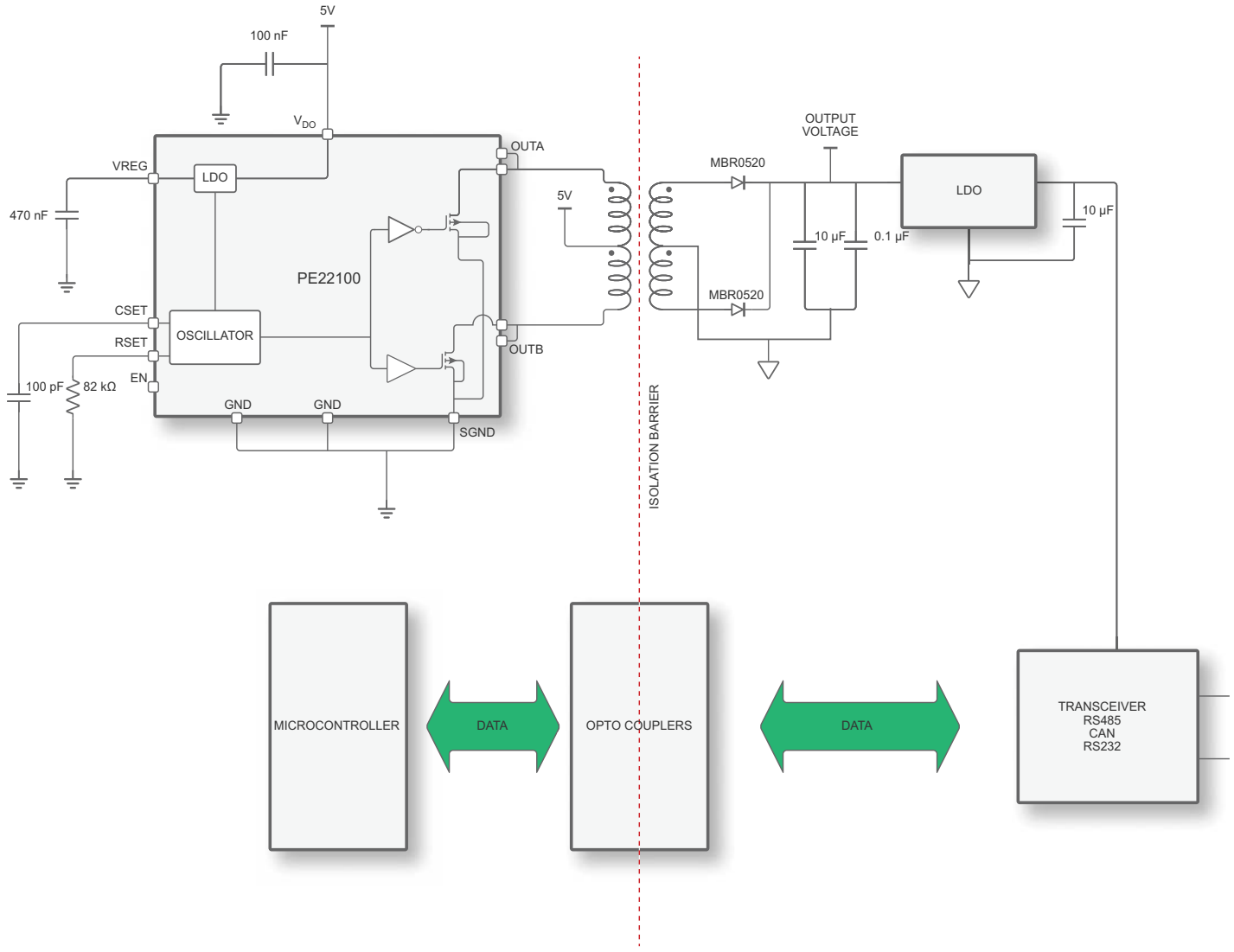
Internally, the PE22100 divides this value by a factor of 2, for an internal oscillator frequency of 375/2 = 187.5 kHz. This is the frequency that drives the output transistors.

The PE22100 can be driven up to rates of 2 MHz at CSET. As CSET is decreased, be sure external PCB stray capacitances do not introduce errors into the oscillator frequency.

Applications Information

The PE22100 often is used to generate isolated supplies for transceivers in isolated interface applications, as shown in **Figure 19**. In this application, the output is further regulated by a linear regulator to provide an isolated regulated supply for the transceivers. The efficiency loss due to the linear regulator should be taken into account for the system efficiency calculation. At low load currents, switching transitions from the primary side can be capacitively coupled to the secondary side. Adding a zener diode across the output voltage will clamp this voltage.

Figure 19 • *Typical Application*



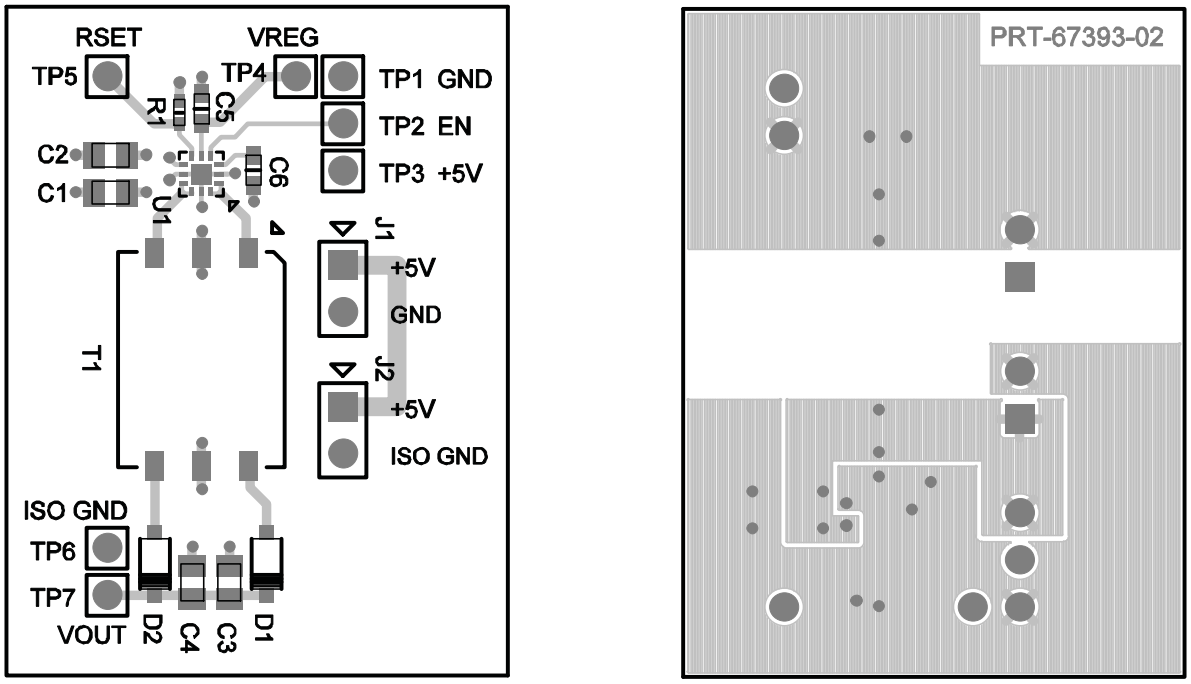
Evaluation Kit

The PE22100 evaluation board (EVB) is designed on a 2.54 mm pitch to allow customers to evaluate the PE22100 on plug board.

The EVB is assembled with a PE22100 driving a 782100/55JVC transformer, which is rectified by D1 and D2 to generate an isolated supply voltage.

To change the operating frequency, replace C6.

Figure 20 • *Evaluation Kit Layout for PE22100*



Pin Information

This section provides pinout information for the PE22100. **Figure 21** shows the pin map of this device for the available package. **Table 7** provides a description for each pin.

Figure 21 • *Pin Configuration (Top View)*

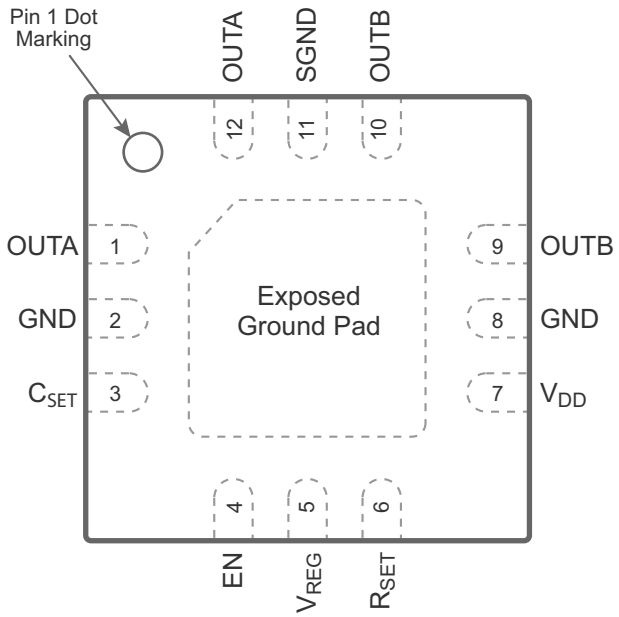


Table 7 • *Pin Descriptions for PE22100*

Pin No.	Pin Name	Description
1, 12	OUTA	Power switch output A connection
2, 8	GND	Ground
3	C_{SET}	Connect an external capacitor to ground to set the oscillator frequency
4	EN	Enable pin active high internally pulled up. Either leave floating or drive a logic low to disable the part. Do not drive EN above V_{REG}.
5	V_{REG}	Internal regulator bypass should be connected to 470 pF to ground
6	R_{SET}	Connect an external 82 kΩ to ground
7	V_{DD}	Positive input for the chip to connect to 3.3V or 5V
9, 10	OUTB	Power switch output B connection
11	SGND	Power FET ground connection is a high power path and should be connected to the same potential as GND
Pad	GND	Exposed pad: ground for proper operation

Packaging Information

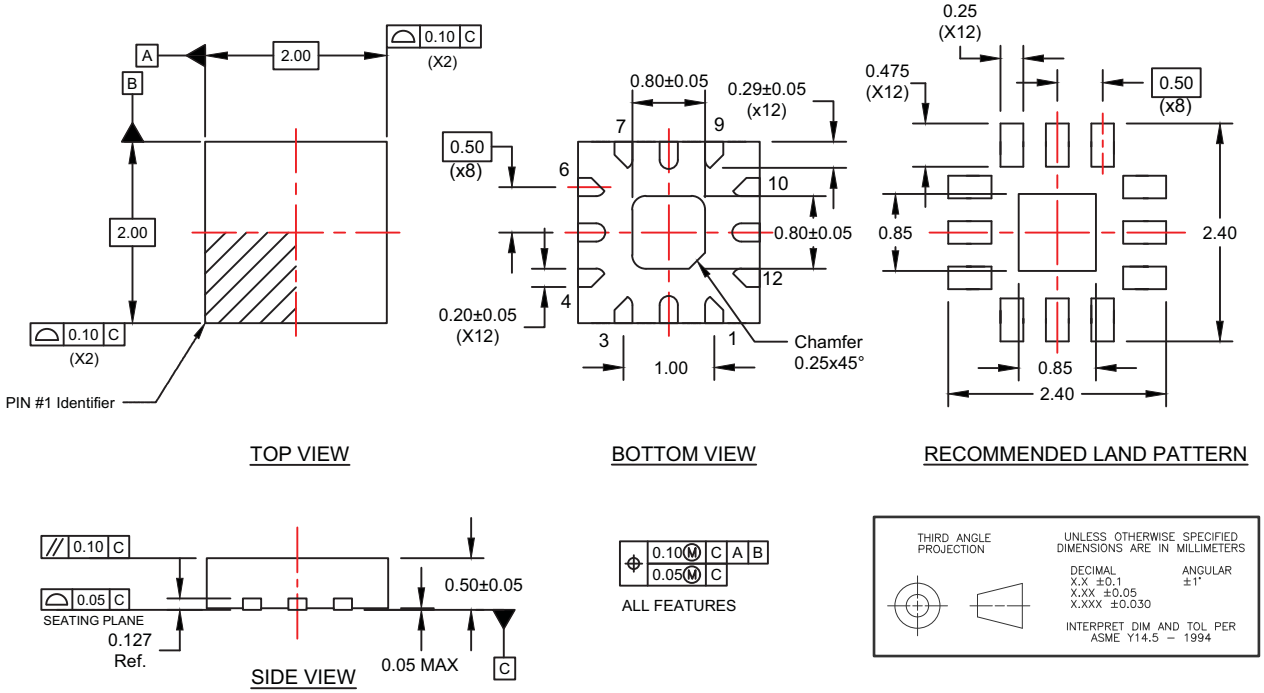
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE22100 in the 2 × 2 × 0.5 mm QFN package is MSL1.

Package Drawing

Figure 22 • *Package Mechanical Drawing for 2 × 2 × 0.5 mm QFN*



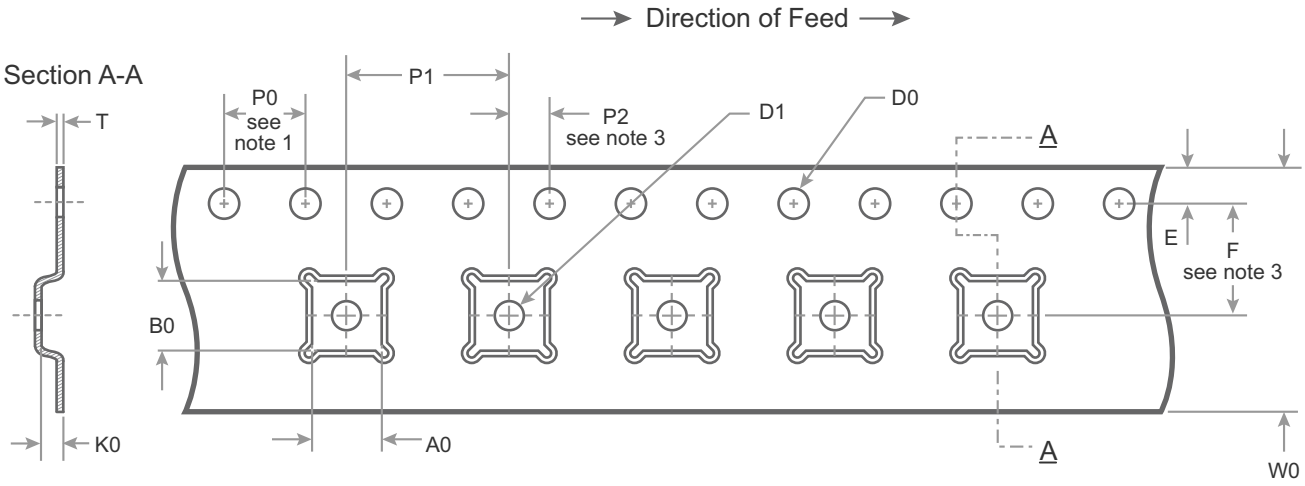
Top-Marking Specification

Figure 23 • *Package Marking Specifications for PE22100*

● = Pin 1 indicator
PP = Alpha code “EK”
YY = Last two digits of assembly year
WW = Assembly work week
ZZ = Assembly lot code (maximum two characters)

Tape and Reel Specification

Figure 24 • *Tape and Reel Specifications for 2 × 2 × 0.5 mm QFN*



A0	2.30
B0	2.30
K0	0.70
D0	2.00 + 0.1/ -0.0
D1	1.0 min
E	1.75 ± 0.10
F	3.50 ± 0.05
P0	4.00
P1	4.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	8.00 ± 0.3

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

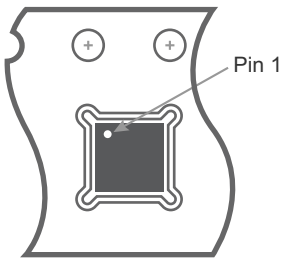
THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030

ANGULAR
±1°

INTERPRET DIM AND TOL PER ASME Y14.5 – 2009



Device Orientation in Tape

Ordering Information

Table 8 lists the available ordering codes for the PE22100 as well as available shipping methods.

Table 8 • *Order Codes for PE22100*

Order Codes	Description	Packaging	Shipping Method
PE22100A-X	PE22100 Transformer driver	2 × 2 mm QFN	500 units/T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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