Using the ACS760 Evaluation Board

Introduction

The ACS760 is a 240 V*A protection IC with integrated hot-swap gate driver and internal 1.5 mΩ Hall effect based current monitor. Complete device description is available on the Allegro® website, www.allegromicro.com. This application note describes the evaluation board supplied by Allegro for demonstrating the capabilities of the ACS760 in various customer applications.

Description

The ACS760 evaluation board only requires a single user-provided 12 V source to power the board and device. For ease of use, on-board banana plugs may be used to connect the 12 V source to the board, and to apply a load.

The on-board A8498 regulator and associated circuitry, located on the back of the evaluation board, is used to provide the second 3.3 V rail. This 3.3 V rail is used for the fault pull-ups as well as to enable the device. To enable the ACS760, a jumper must be placed between +3.3 V and EN on the Molex connector.

To provide a more friendly customer interface, LEDs located on the top of the board will light for fault condition output signals on the OPDLY, OCDLY, FAULT, and S1SHORT pins. Test points are also provided for the following pins: EN, VIOUT, ISET, CG, OCDLY, OPDLY, FAULT, S1FAULT, GND, and GATE. These inputs and outputs are described in the Terminal List table on the next page.

This evaluation board also gives the customer the ability to configure the ACS760 to operate in pure current mode. To do so, place a shunt across jumper J2. This shorts the OPDLY pin to GND, allowing the I_{PF} upper trip level to be set by adjusting the resistor connected between the ISET pin and GND.

The typical component values are shown in the ACS760 evaluation board schematic (figure 3). A pin-out diagram and Terminal List table is provided. In addition to the information found in the datasheet, a fault description table is included below.

For additional information, please contact your local Allegro field application office.

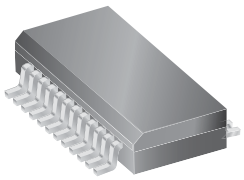
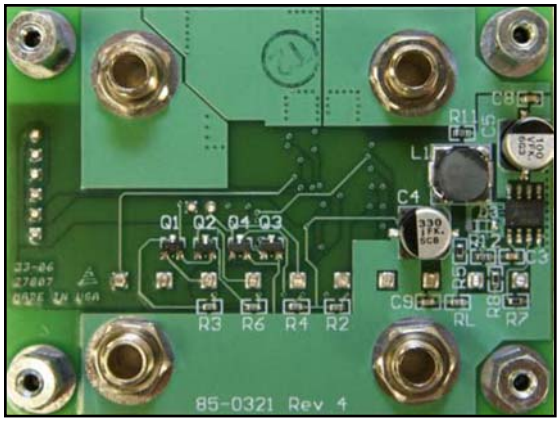


Figure 1. The Allegro ACS760 is provided in a compact, 24-pin QSOP package

(A)



(B)

Figure 2. The Allegro ACS760 Evaluation board. A: top side, with test points and LEDs. B: bottom side.

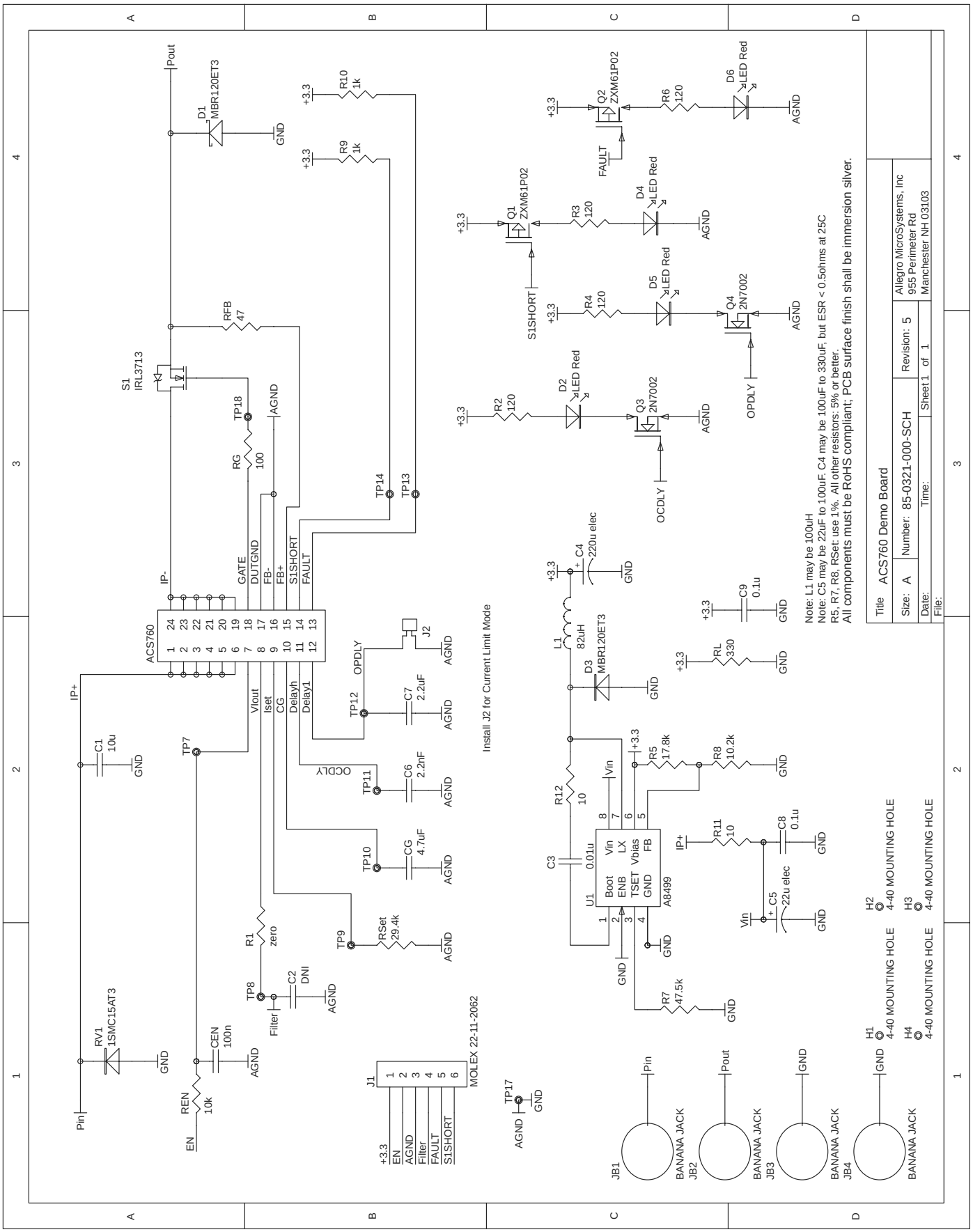


Figure 3. The Allegro ACS760 Evaluation board schematic diagram

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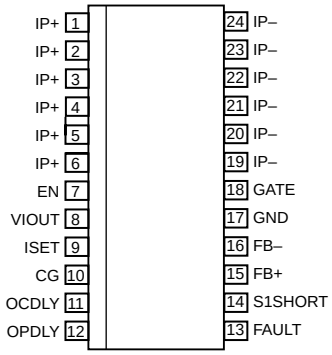
Pin-out Diagram



Terminal List Table

Number	Name	Function
1-6	IP+	Primary sensed current conduction path input; power input pins: connected to V_{CC}
7	EN	Enable pin. Toggling this pin to the low state after a FAULT condition resets the ACS760.
8	VIOUT	Analog current sense output. Output voltage on this pin is proportional to the current flowing from the IP+ pins to the IP– pins.
9	ISET	Terminal for R_{SET} resistor. Sets Fault Current Threshold, I_{PF}, via external resistor, R_{SET}, connected between this terminal and GND. Factory trimmed 100 µA current source flows out of this pin.
10	CG	Terminal for C_G capacitor. May be used to adjust the turn-on time and soft start control of an external MOSFET, S1. Voltage on this pin limits inrush current through MOSFET S1. Set via external capacitance, C_G, connected between this pin and GND. This capacitor is charged by an internal 20 µA current source.
11	OCDLY	Terminal for external capacitor, C_{OCD}, Used to adjust delay for overcurrent shutdown, set via the external capactior, C_{OCD}, connected between this pin and GND.
12	OPDLY	Terminal for external capacitor, C_{OPD}, Used to adjust delay for overpower shutdown, set via the external capactior, C_{OPD}, connected between this pin and GND.
13	FAULT	Active low; output signal for short circuit and 240 V*A overload faults; does not trip for S1 short circuit fault. Connect a 1 kΩ pull-up resistor between this pin and the 3.3 V rail.
14	S1SHORT	Active low; output signal for MOSFET S1 failure. Connect a 1 kΩ pull-up resistor between this pin and the 3.3 V rail.
15	FB+	Input of positive feedback on output voltage. Used to determine 240 V*A threshold by difference between FB+ and FB– pins.
16	FB-	Input of negative feedback on output voltage. Used to determine 240 V*A threshold by difference between FB+ and FB– pins. Pulling the FB– pin to 3.3 V, and the OPDLY pin to GND, disables the 240 V*A power fault, which allows the ACS760 to operate purely in Current Mode.
17	GND	Terminal for ground connection.
18	GATE	Terminal for external MOSFET, S1. Provides output voltage to drive S1. Current through S1 is controlled at start-up by external capacitance connected between the CG pin and GND.
19-24	IP–	Primary sensed current conduction path output; power output pins.

Fault Description Table

240 V*A Power Fault	IpF Fault (Soft Short)	Overcurrent Fault (Hard Short)	S1 Short
–FAULT pin falls low when power supply load > 240 V*A –Adding an external cap from OCPDLY to GND adjusts delay for over-power shutdown	–User may set IpF fault current threshold (nominally 30 to 40 A) via resistor from ISET pin to GND –FAULT pin falls low when current exceeds IpF fault current threshold –Adding an external cap from the OCDLY pin to GND adjusts the delay for overcurrent shutdown	–50 mΩ load to GND –The ACS760 pulls down the external MOSFET gate approximately 2 µs after the load current exceeds the overcurrent fault threshold	–If the gate on the external MOSFET is low and more than 2.1 A flows through the ACS760, the S1SHORT signal pin falls to the low state –Unlike the 240 V*A Power fault, IpF fault, and Overcurrent fault, the EN pin may not be cycled to reset the S1 Short signal; power to the device must be cycled

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