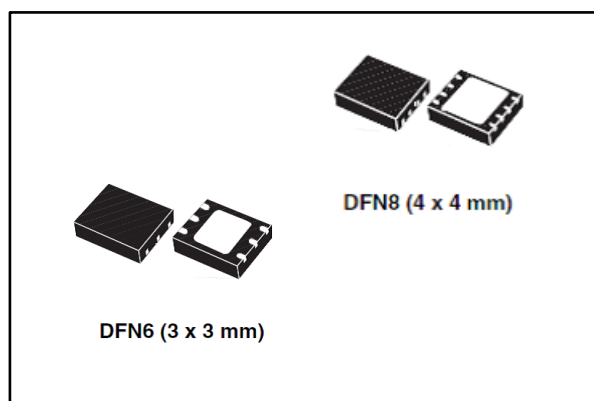


2 A high PSRR ultra low drop linear regulator with reverse current protection

Datasheet - production data



Features

- Input voltage from 1.25 V to 6.0 V
- Ultra low drop: 130 mV (typ.) at 2 A load
- 1% output accuracy at 25 °C, 2% in full temperature range
- High PSRR: 70 dB at 1 kHz
- Reverse current protection
- 2 A guaranteed output current
- Available in fixed and adjustable output voltage version from 0.5 V with 100 mV step
- Power Good
- Internal current and thermal limit
- Operating junction temperature range: -40 °C to 125 °C
- DFN6 (3 x 3 mm) and DFN8 (4 x 4 mm) packages

Applications

- Telecom infrastructure
- Medium power POL

Description

The LD39200 provides 2 A of maximum current with an input voltage range from 1.25 V to 6.0 V, and a typical dropout voltage of 130 mV.

It is stable with ceramic capacitors on the output (10 µF).

Typical power supply rejection ratio is 70 dB at 1 kHz and starts to roll off at 20 kHz.

The enable logic control function puts the LD39200 in shutdown mode, reducing the total current consumption to 10 nA (typ.).

Power Good flag is available on a dedicated pin.

The device also includes reverse current protection, short-circuit constant current limit and thermal protection.

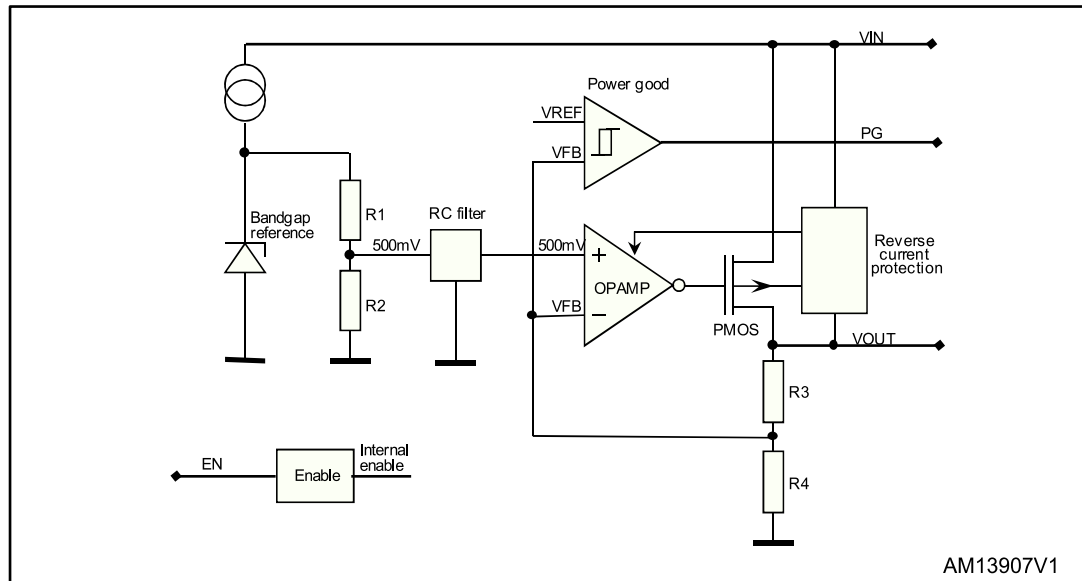
Typical applications are for Telecom infrastructure and consumer.

Contents

1	Block diagram.....	3
2	Pin configuration and description.....	4
3	Typical application	6
4	Maximum ratings	7
5	Electrical characteristics	8
6	Application information	12
	6.1 Thermal and short-circuit protections	12
	6.2 Output voltage setting for ADJ version.....	12
	6.3 Enable pin	12
	6.4 Power Good pin (PG).....	12
	6.5 Reverse current protection	13
7	Typical performance characteristics	14
8	Package mechanical data	19
	8.1 DFN6 (3 x 3 mm) mechanical data.....	20
	8.2 DFN8 (4 x 4 mm) mechanical data.....	22
9	Packaging mechanical data.....	24
	9.1 DFN6 (3 x 3 mm) tape and reel mechanical data.....	24
	9.2 DFN8 (4 x 4 mm) reel mechanical data.....	26
10	Ordering information.....	28
11	Revision history	29

1 Block diagram

Figure 1: Block diagram



2 Pin configuration and description

Figure 2: Pin configuration (top view)

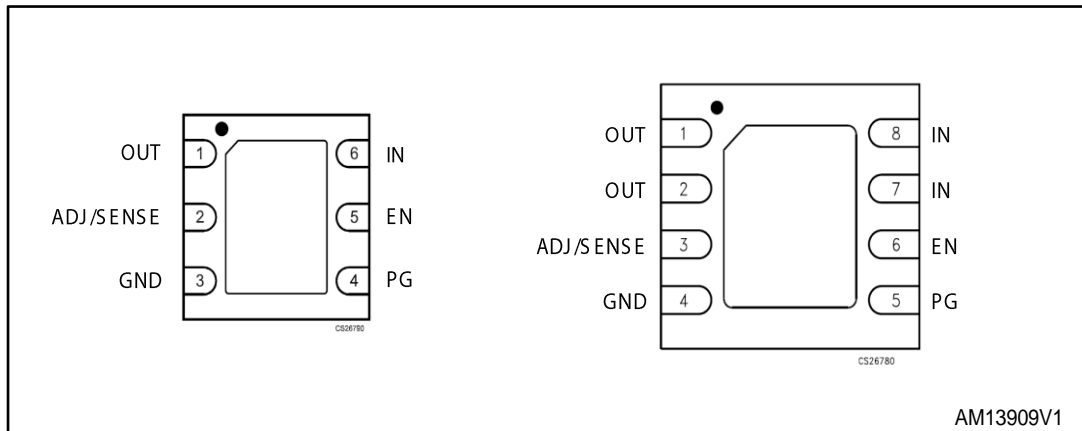


Table 1: DFN6 (3 x 3 mm) package pin description

Pin name	Pin number	Description
IN	6	Input voltage
GND	3	Ground
EN	5	Enable pin. The device is in OFF state when this pin is pulled low
ADJ/sense ⁽¹⁾	2	Adjustable pin on ADJ version can be connected to external resistor divider to set the output voltage. Output sense pin on the fixed version has to be connected to V_{OUT}
OUT	1	Output voltage
PG	4	Power Good
GND	Exposed pad	Exposed pad should be connected to GND

Notes:

⁽¹⁾The output sense pin of the fixed version has to be connected to the output pin for proper operation.

Table 2: DFN8 (4 x 4 mm) package pin description

Pin name	Pin number	Description
IN ⁽¹⁾	7, 8	Input voltage
GND	4	Ground
EN	6	Enable pin. The device is in OFF state when this pin is pulled low
ADJ/sense ⁽²⁾	3	Adjustable pin on ADJ version can be connected to external resistor divider to set the output voltage. Output sense pin on the fixed version has to be connected to V _{OUT}
OUT ⁽³⁾	1, 2	Output voltage
PG	5	Power Good
GND	Exposed pad	Exposed pad should be connected to GND

Notes:

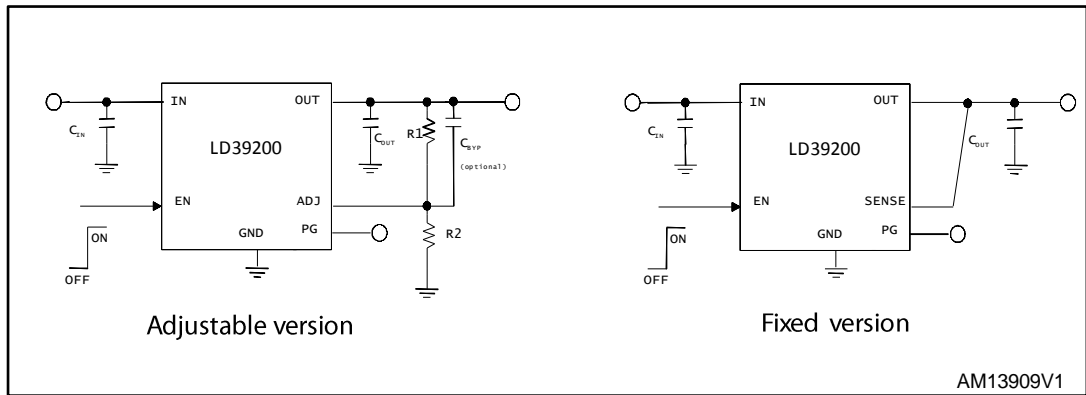
⁽¹⁾Both of input pins have to be connected together on the board.

⁽²⁾The output sense pin of the fixed version has to be connected to the OUT pin for proper operation.

⁽³⁾Both of output pins have to be connected together on the board.

3 Typical application

Figure 3: LD39200 typical application schematic



R1 and R2 are calculated according to the following formula: $R1 = R2 \times (V_{OUT} / V_{ADJ})$. Recommended value for C_{IN} and C_{OUT} is 10 μ F.

4 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 7	V
V_{ADJ}	Adjustable voltage	-0.3 to 2	V
V_{OUT}/V_{SENSE}	Output voltage/output sense voltage	-0.3 to 7	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	-0.3 to 7	V
PG	Power Good pin voltage	-0.3 to 7	V
P_D	Power dissipation	Internally limited	W
ESD	Charge device model	± 500	V
	Human body model	± 2000	
T_{J-OP}	Operating junction temperature	-40 to 125	$^{\circ}C$
T_{J-MAX}	Maximum junction temperature	150	$^{\circ}C$
T_{STG}	Storage temperature	-55 to 150	$^{\circ}C$



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4: Thermal data

Symbol	Parameter	DFN6 (3 x 3 mm)	DFN8 (4 x 4 mm)	Unit
R_{THJC}	Junction-to-case thermal resistance	10	4	$^{\circ}C/W$
R_{THJA}	Junction-to- ambient thermal resistance	55	40	

5 Electrical characteristics

($T_J = 25\text{ °C}$, $V_{IN} = V_{OUT} + 1\text{ V}$; $V_{OUT} = V_{ADJ}$; $C_{IN} = 10\text{ }\mu\text{F}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $V_{EN} = V_{IN}$)

Table 5: Electrical characteristics, adjustable version

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		1.25		6.0	V
V_{ADJ}	Adjustable pin voltage			0.5		V
	Adjustable pin voltage accuracy	$T_J = 25\text{ °C}$ $-40\text{ °C} < T_J < 125\text{ °C}$	-1.0 -2.0		1.0 2.0	%
I_{ADJ}	Adjustable pin current	$-40\text{ °C} < T_J < 125\text{ °C}$		100		nA
$DV_{ADJ}\%/DV_{IN}$	Static line regulation	$V_{OUT} + 1\text{ V} < V_{IN} < 6.0\text{ V}$; $T_J = 25\text{ °C}$		0.01		% / V
		$-40\text{ °C} < T_J < 125\text{ °C}$			0.2	
$DV_{ADJ}\%/DI_{OUT}$	Static load regulation	$0\text{ mA} < I_{OUT} < 2\text{ A}$; $T_J = 25\text{ °C}$		0.1		% / A
		$-40\text{ °C} < T_J < 125\text{ °C}$			0.4	
V_{DROP}	Dropout voltage ⁽¹⁾	$V_{IN} = 1.4\text{ V}$; $I_{OUT} = 1\text{ A}$; $-40\text{ °C} < T_J < 125\text{ °C}$		120	250	mV
		$V_{IN} = 2.5\text{ V}$; $I_{OUT} = 2\text{ A}$; $-40\text{ °C} < T_J < 125\text{ °C}$		135	250	
		$V_{IN} = 5.3\text{ V}$; $I_{OUT} = 2\text{ A}$; $-40\text{ °C} < T_J < 125\text{ °C}$		110	250	
eN	Output noise voltage	$V_{OUT} = V_{ADJ}$; $f = 10\text{ Hz to } 100\text{ kHz}$		45		μV_{RMS} / V_{OUT}
eN	Output noise voltage	$V_{IN} = V_{OUT} + 0.4\text{ V}$; $I_{OUT} = 700\text{ mA}$; $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$; $R2 = 10\text{ k}\Omega$; $R1 = (V_{OUT} - 0.5) \times 20\text{ k}\Omega$; $C_{byp} = 470\text{ nF}$		24		μV_{RMS}
SVR	Supply voltage rejection	$V_{OUT} = 1.8\text{ V}$; $V_{IN} = V_{OUT} + 0.5\text{ V}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $T_J = 25\text{ °C}$; $f = 1\text{ kHz}$		70		dB
		$V_{OUT} = 1.8\text{ V}$; $V_{IN} = V_{OUT} + 0.5\text{ V}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $T_J = 25\text{ °C}$; $f = 100\text{ kHz}$		50		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		$V_{OUT} = 1.8 \text{ V};$ $V_{IN} = V_{OUT} + 0.5 \text{ V};$ $C_{OUT} = 10 \text{ } \mu\text{F};$ $I_{OUT} = 10 \text{ mA}; T_J = 25 \text{ } ^\circ\text{C};$ $f = 500 \text{ kHz}$		50		dB
		$V_{OUT} = 1.8 \text{ V};$ $V_{IN} = V_{OUT} + 0.5 \text{ V};$ $C_{OUT} = 10 \text{ } \mu\text{F};$ $I_{OUT} = 10 \text{ mA}; T_J = 25 \text{ } ^\circ\text{C};$ $f = 1 \text{ MHz}$		40		
I_Q	Quiescent current	$I_{OUT} = 0 \text{ A}$		100		μA
		$I_{OUT} = 0 \text{ A};$ $-40 \text{ } ^\circ\text{C} < T_J < 125 \text{ } ^\circ\text{C}$			300	
		$I_{OUT} = 2 \text{ A};$		1		mA
		$I_{OUT} = 2 \text{ A};$ $-40 \text{ } ^\circ\text{C} < T_J < 125 \text{ } ^\circ\text{C}$			3	
	Shutdown current	$V_{EN} = 0, V_{IN} = 6 \text{ V}$		10		nA
I_{SC}	Short-circuit current	$V_{OUT} = 0 \text{ V}$		3.5		A
I_{MIN}	Minimum output current				0	A
V_{EN}	Enable input logic low	$1.25 \text{ V} < V_{IN} < 6.0 \text{ V}$ $-40 \text{ } ^\circ\text{C} < T_J < 125 \text{ } ^\circ\text{C}$			0.5	V
	Enable input logic high		1.2			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN};$ $1.25 < V_{IN} < 6.0 \text{ V}$		10		nA
PG	Power Good output threshold	Rising edge		$0.92^* V_{out}$		V
		Falling edge		$0.8^* V_{out}$		
	Power Good output voltage low	$I_{sink} = 6 \text{ mA}$ open drain output			0.4	
T_{SHDN}	Thermal shutdown			170		$^\circ\text{C}$
	Hysteresis			20		

Notes:

⁽¹⁾ Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value; this specification does not apply to nominal output voltages below 1.2 V.

(T_J = 25 °C, V_{IN} = V_{OUT}+1 V; C_{IN} = 10 μF; C_{OUT} = 10 μF; I_{OUT} = 10 mA; V_{EN} = V_{IN})

Table 6: Electrical characteristics, fixed version

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IN}	Operating input voltage range		1.25		6.0	V
V _{OUT}	Output voltage accuracy	T _J = 25 °C	-1.0		1.0	%
		-40 °C < T _J < 125 °C	-2.0		2.0	
D _{VADJ%} / D _{VIN}	Static line regulation	V _{OUT} + 1 V < V _{IN} < 6.0 V; T _J = 25 °C		0.01		% / V
		-40 °C < T _J < 125 °C			0.1	
D _{VADJ%} / D _{IOUT}	Static load regulation	0 mA < I _{OUT} < 2 A; T _J = 25 °C		0.05		% / A
		-40 °C < T _J < 125 °C			0.4	
V _{DROP}	Dropout voltage	V _{OUT} = 3.3 V; I _{OUT} = 2 A; -40 °C < T _J < 125 °C		130	250	mV
eN	Output noise voltage	V _{OUT} = 2.5 V; f = 10 Hz to 100 kHz;		40		μV _{RMS} / V _{OUT}
SVR	Supply voltage rejection	V _{OUT} = 1.8 V; V _{IN} = V _{OUT} + 0.5 V; C _{OUT} = 10 μF; I _{OUT} = 10 mA; T _J = 25 °C; f = 1 kHz		70		dB
		V _{OUT} = 1.8 V; V _{IN} = V _{OUT} + 0.5 V; C _{OUT} = 10 μF; I _{OUT} = 10 mA; T _J = 25 °C; f = 100 kHz		50		
		V _{OUT} = 1.8 V; V _{IN} = V _{OUT} + 0.5 V; C _{OUT} = 10 μF; I _{OUT} = 10 mA; T _J = 25 °C; f = 500 kHz		50		
		V _{OUT} = 1.8 V; V _{IN} = V _{OUT} + 0.5 V; C _{OUT} = 10 μF; I _{OUT} = 10 mA; T _J = 25 °C; f = 1 MHz		40		
I _Q	Quiescent current	I _{OUT} = 0 A		100		μA
		I _{OUT} = 0 A; -40 °C < T _J < 125 °C			300	
		I _{OUT} = 2 A;		1		mA
		I _{OUT} = 2 A; -40 °C < T _J < 125 °C			3	
	Shutdown current	V _{en} = 0, V _{in} = 6 V		50		nA
I _{SC}	Short-circuit current	V _{OUT} = 0 V		3.5		A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{MIN}	Minimum output current				0	A
V_{EN}	Enable input logic low	1.25 V < V_{IN} < 6.0 V -40 °C < T_J < 125 °C			0.5	V
	Enable input logic high		1.2			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$; 1.25 < V_{IN} < 6.0 V		10		nA
PG	Power Good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power Good output voltage low	$I_{sink} = 6$ mA open drain output			0.4	
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			20		

6 Application information

6.1 Thermal and short-circuit protections

The LD39200 is self-protected from short-circuit conditions and overtemperature. When the output load is higher than the one supported by the device, the output current rises until the limit of typically 3.5 A is reached; at this point the current is kept constant even when the load impedance is zero. The thermal protection acts when the junction temperature reaches 170 °C. The IC enters the shutdown status. As soon as the junction temperature falls again below 150 °C the device starts working again. In order to calculate the maximum power the device can dissipate, keeping the junction temperature below T_{J-OP} , the following formula is used:

Equation 1

$$P_{DMAX} = (125 - T_{AMB}) / R_{THJ-A}$$

6.2 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.5 V up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, allowing remote voltage sensing. The resistor divider can be selected using the following equation:

Equation 2

$$V_{OUT} = V_{ADJ} (1 + R1 / R2), \text{ with } V_{ADJ} = 0.5 \text{ V (typ.)}$$

6.3 Enable pin

The LD39200 features an enable function. When the EN voltage is higher than 1.2 V the device is ON, and if it is lower than 0.5 V the device is OFF. In shutdown mode, the total current consumption is 10 nA (typ). The EN pin does not have an internal pull-up, therefore it cannot be left floating if it is not used.

6.4 Power Good pin (PG)

Some applications require a flag showing that the output voltage is in the correct range. Power Good threshold depends on the output voltage. When the output voltage is higher than $0.92 \cdot V_{OUT(nom)}$, the PG pin goes to high impedance. If the output voltage is below $0.80 \cdot V_{OUT(nom)}$ the PG pin goes to low impedance. If the device works well, the PG pin is at high impedance.

6.6 Reverse current protection

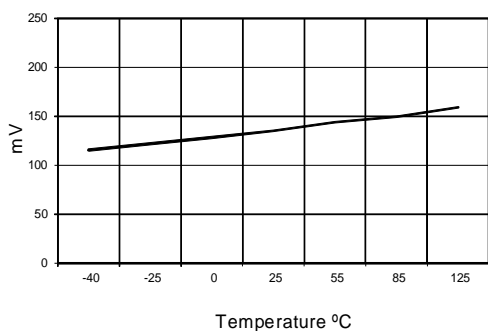
The device avoids the reverse current to flow from the output to the input during any operating condition ($EN=0$ or $EN=1$, $V_{IN}>V_{OUT}+V_{DROP}$). During fast turn-on/off this function prevents a big current from flowing to the input. Moreover it is used to avoid the reverse current to flow from the output pin to the input one, when other power supplies, providing a voltage higher than the input voltage, are connected to the output pin. If a power supply, providing a voltage lower than LDO output voltage, is connected to OUT pin, LDO works in current protection, causing high power dissipation inside the device.

When the device is disabled ($EN=low$) and $V_{OUT}>0$ V, a small current (few μA) is sunk from the OUT pin.

7 Typical performance characteristics

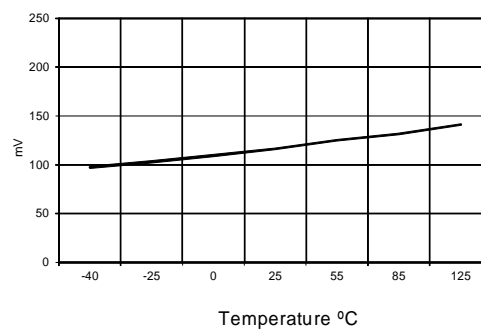
(The following plots are referred to the typical application circuit and, unless otherwise noted, at $T_A = 25\text{ }^\circ\text{C}$)

Figure 4: Dropout voltage vs temperature
($V_{in} = 1.3\text{ V}$, $I_{out} = 1\text{ A}$)



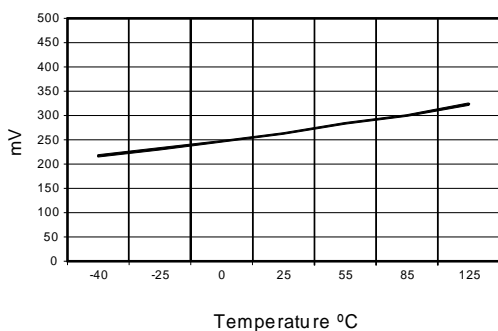
AM13910V1

Figure 5: Dropout voltage vs temperature
($V_{in} = 1.4\text{ V}$, $I_{out} = 1\text{ A}$)



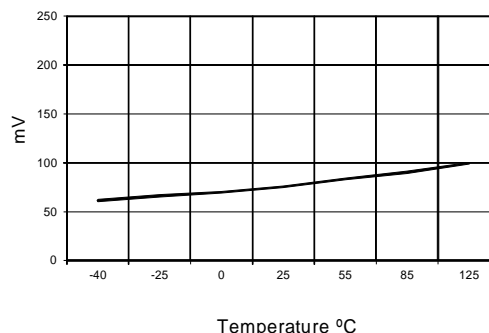
AM13911V1

Figure 6: Dropout voltage vs temperature
($V_{in} = 1.4\text{ V}$, $I_{out} = 2\text{ A}$)



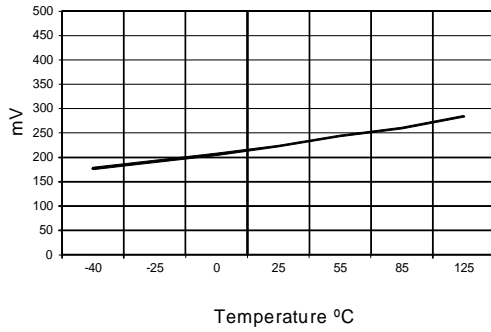
AM13912V1

Figure 7: Dropout voltage vs temperature
($V_{in} = 1.5\text{ V}$, $I_{out} = 1\text{ A}$)



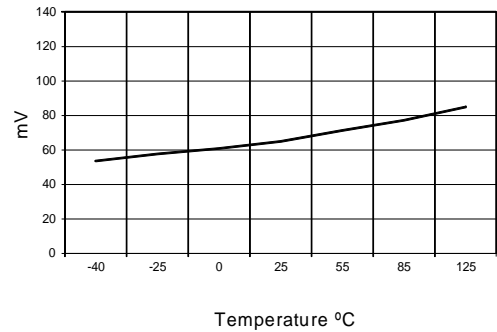
AM13913V1

Figure 8: Dropout voltage vs temperature
($V_{in} = 1.5\text{ V}$, $I_{out} = 2\text{ A}$)



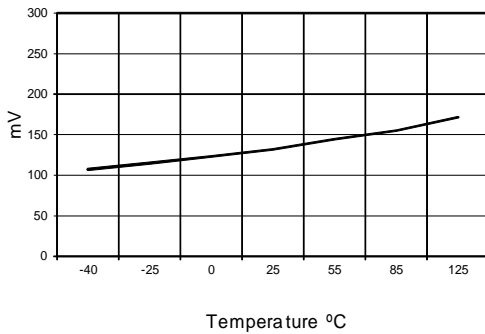
AM13914V1

Figure 9: Dropout voltage vs temperature
($V_{in} = 2.5\text{ V}$, $I_{out} = 1\text{ A}$)



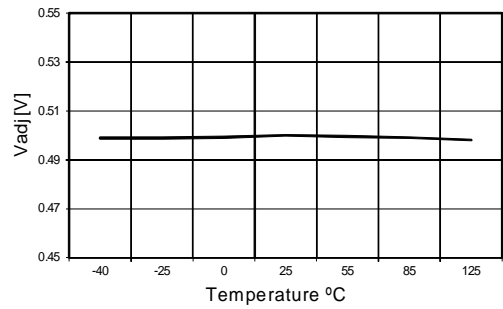
AM13915V1

Figure 10: Dropout voltage vs temperature
($V_{in} = 2.5\text{ V}$, $I_{out} = 2\text{ A}$)



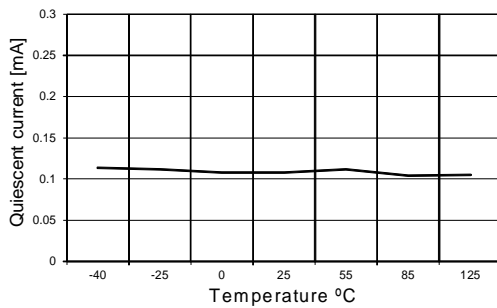
AM13916V1

Figure 11: Reference voltage vs temperature
($V_{in} = 1.5\text{ V}$, $I_{out} = 10\text{ mA}$)



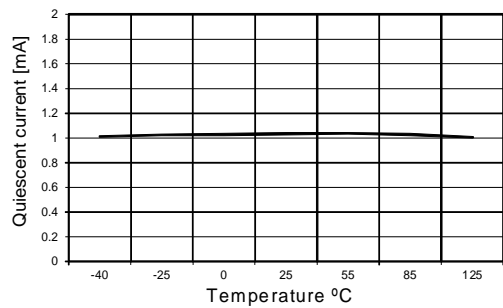
AM13917V1

Figure 12: Quiescent current vs temperature
($V_{in} = 1.5\text{ V}$, $I_{out} = 0\text{ mA}$)



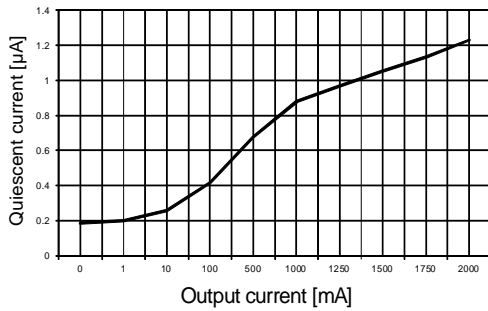
AM13918V1

Figure 13: Quiescent current vs temperature
($V_{in} = 1.5\text{ V}$, $I_{out} = 2\text{ A}$)



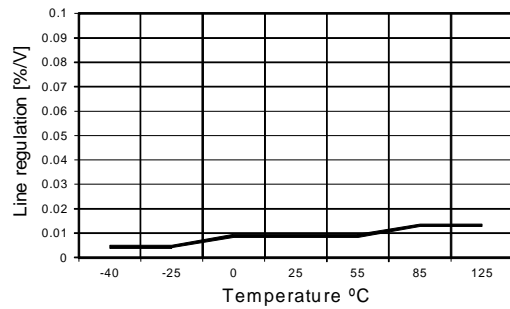
AM13919V1

Figure 14: Quiescent current vs output current



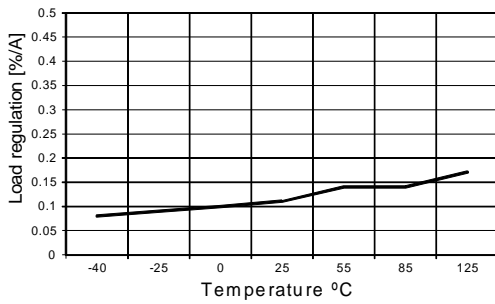
AM13920V2

Figure 15: Line regulation vs temperature (1.5 V ≤ Vin ≤ 6 V, Iout = 10 mA)



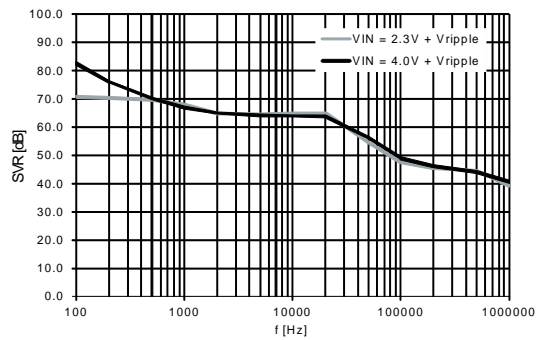
AM13920V1

Figure 16: Load regulation vs temperature (Vin = 1.5 V, 0 < Iout < 2 A)



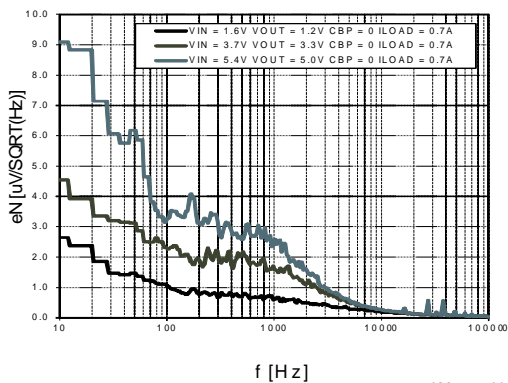
AM13921V1

Figure 17: SVR vs frequency



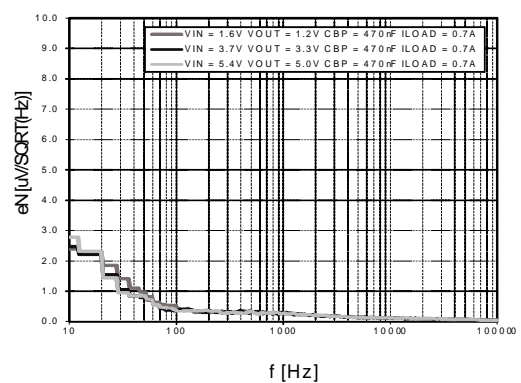
AM13922V1

Figure 18: Noise spectral density (no Cbyp)



AM13923V1

Figure 19: Noise spectral density (Cbyp = 470 nF)



AM13924V1

Figure 20: Stability plan

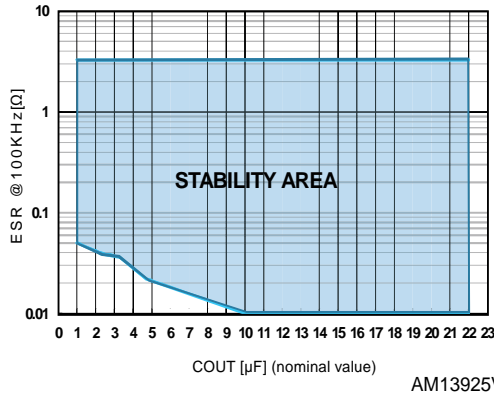


Figure 21: Enable startup, $V_{in} = 1.25\text{ V}$, $I_{out} = 2\text{ A}$

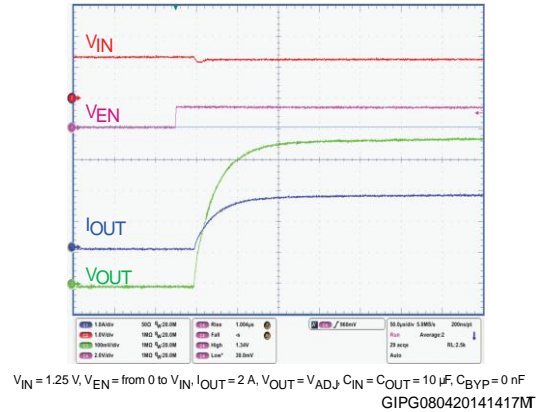


Figure 22: Enable startup, $V_{in} = 6\text{ V}$, $I_{out} = 2\text{ A}$

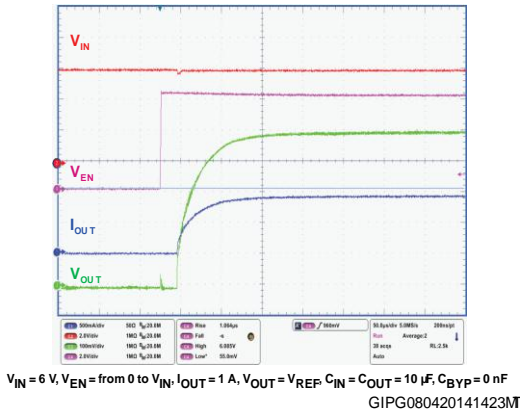


Figure 23: Enable startup, no Cbyp

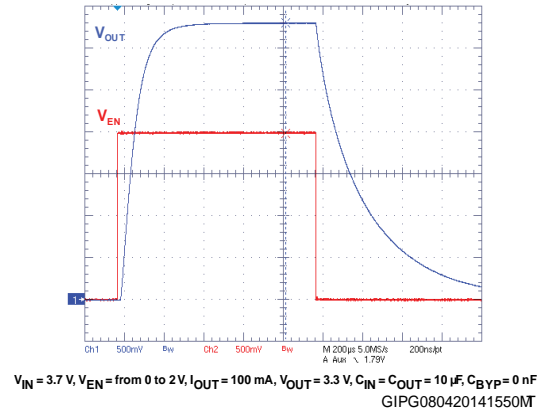


Figure 24: Enable startup, $C_{byp} = 470\text{ nF}$

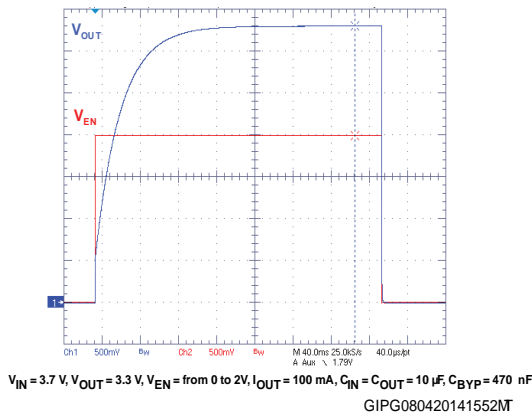


Figure 25: Line transient

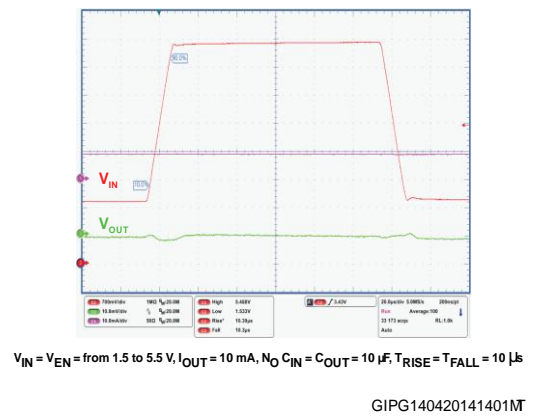
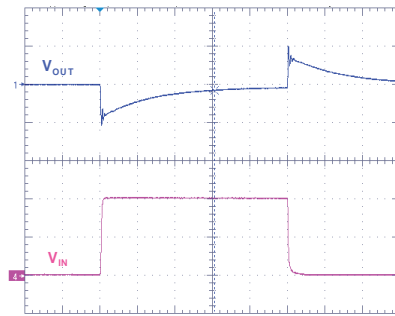


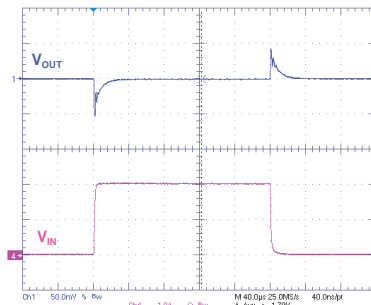
Figure 26: Load transient, no Cbyp



$V_{IN} = 3.7\text{ V}, V_{OUT} = 3.3\text{ V}, I_{LOAD} = 10\text{ mA to } 2\text{ A}, C_{BYP} = 0\text{ nF}$

GIPG140420141403M

Figure 27: Load transient, Cbyp = 470 nF



$V_{IN} = 3.7\text{ V}, V_{OUT} = 3.3\text{ V}, I_{LOAD} = 10\text{ mA to } 2\text{ A}, C_{BYP} = 470\text{ nF}$

GIPG140420141405M

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

8.1 DFN6 (3 x 3 mm) mechanical data

Figure 28: DFN6 (3 x 3 mm) drawings

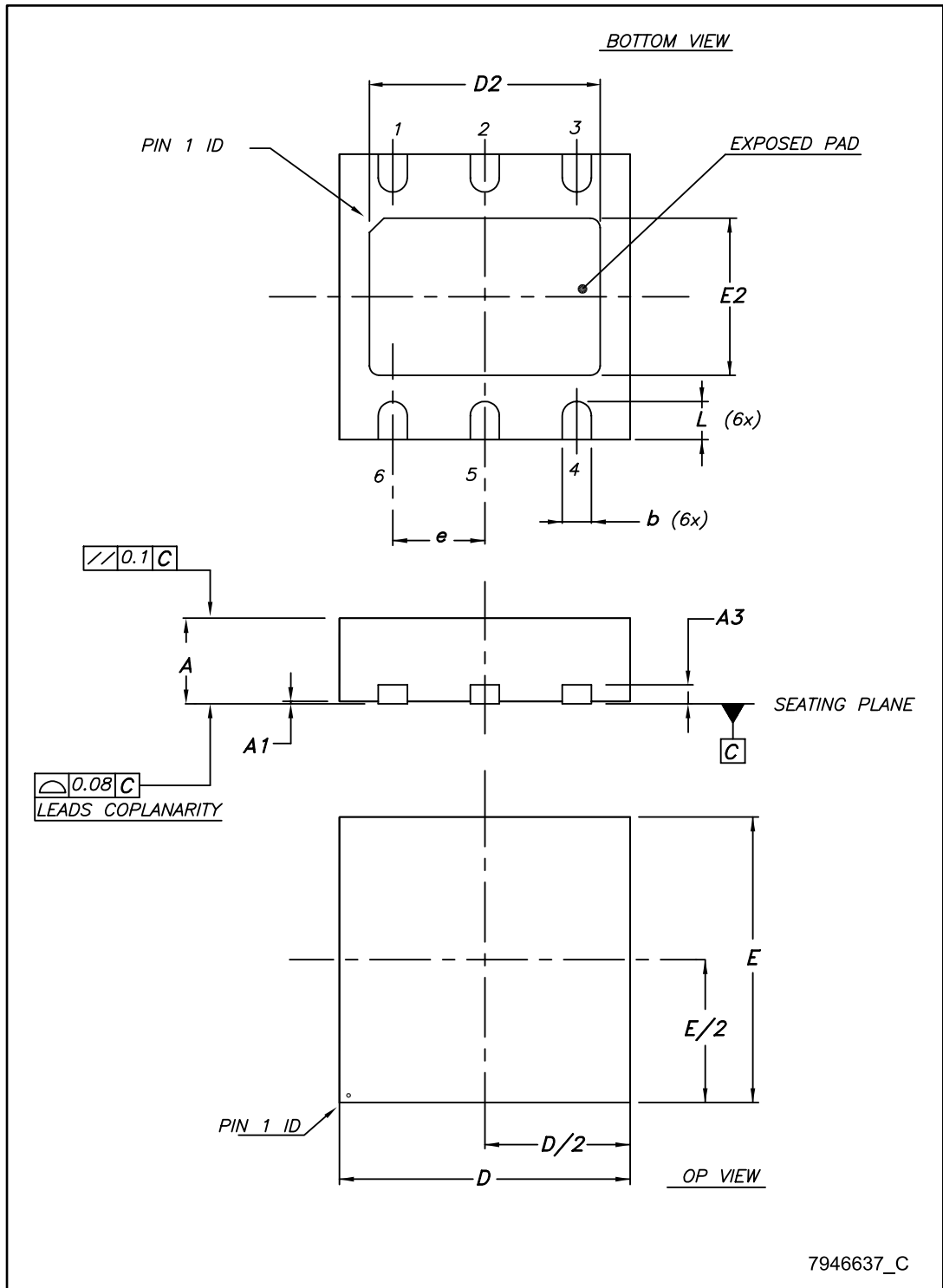
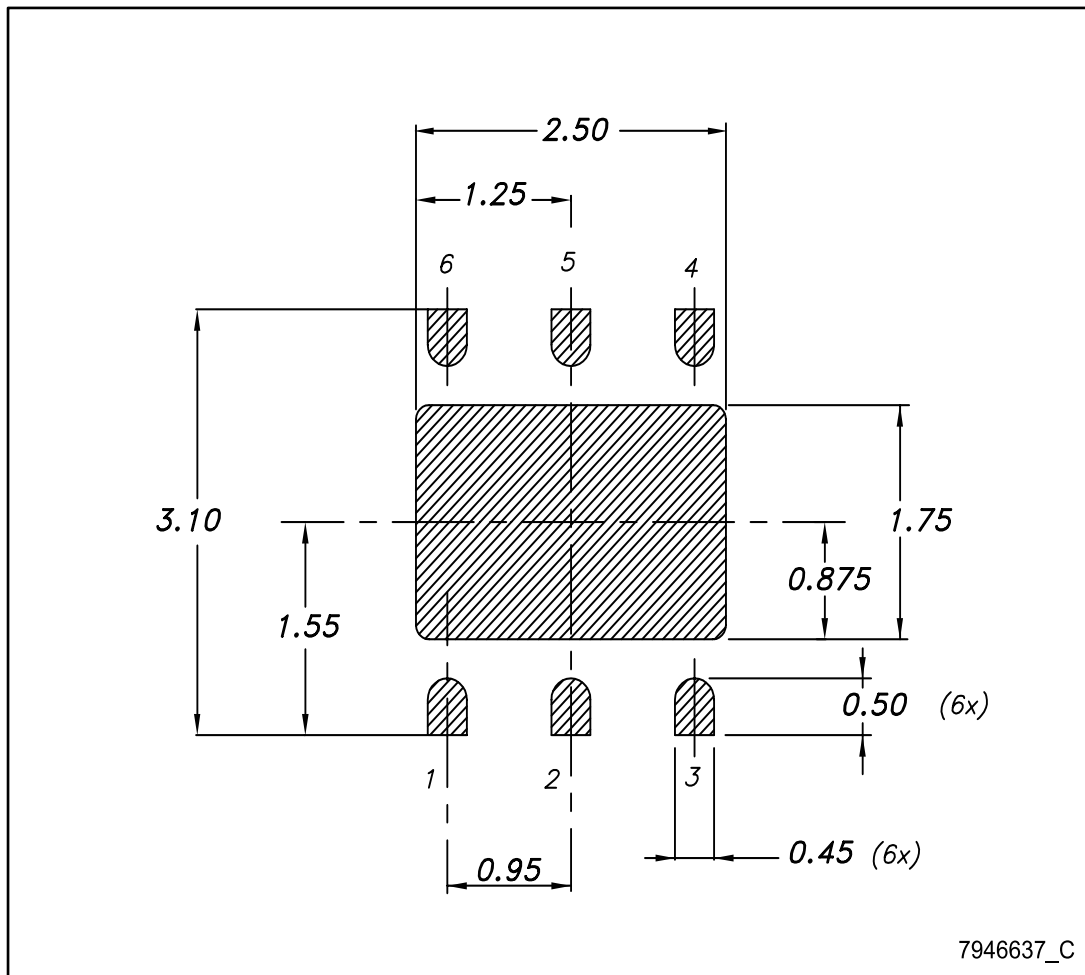


Table 7: DFN6 (3 x 3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 29: DFN6 (3 x 3 mm) footprint (all dimensions are in mm)



8.2 DFN8 (4 x 4 mm) mechanical data

Figure 30: DFN8 (4 x 4 mm) drawing

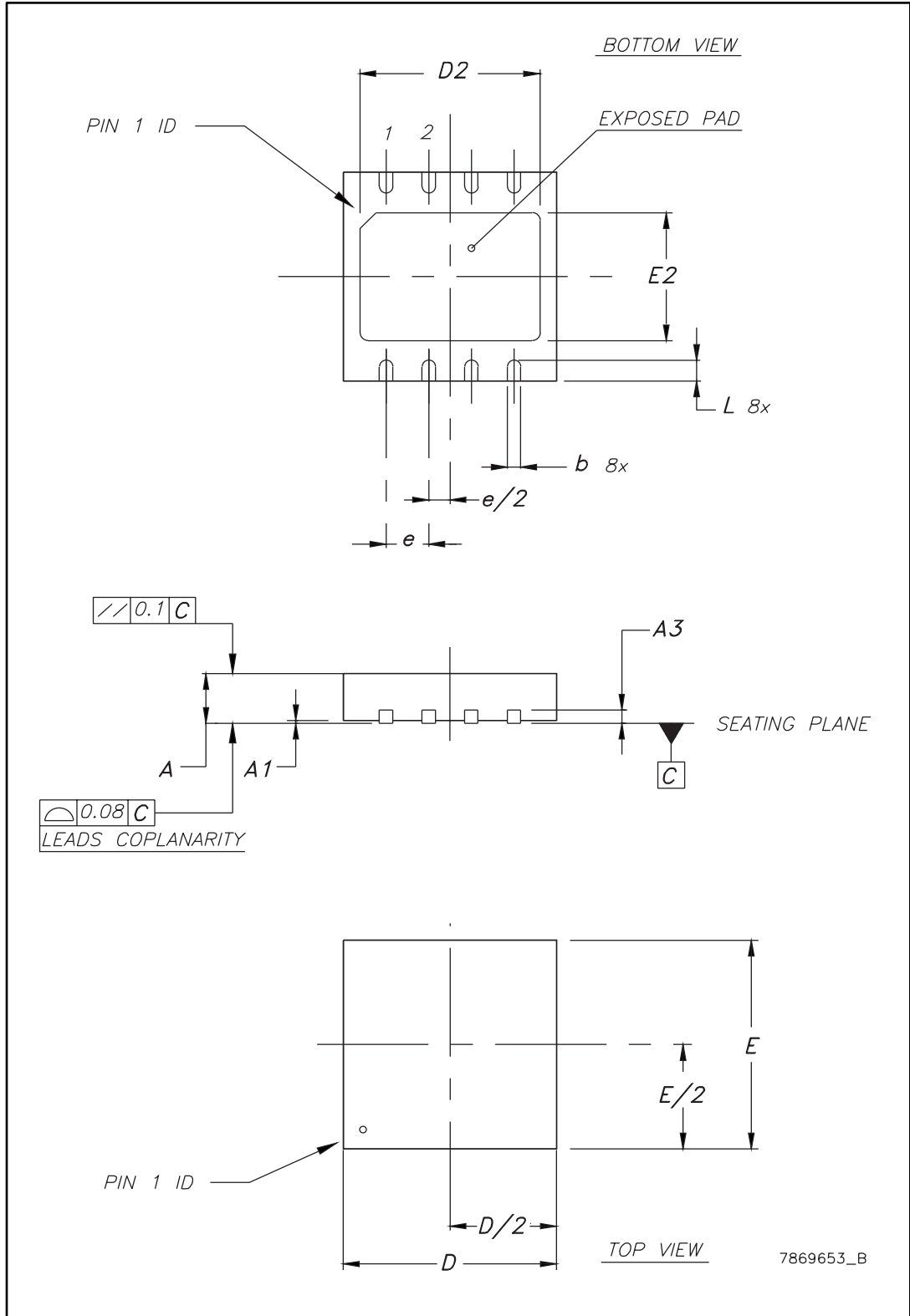
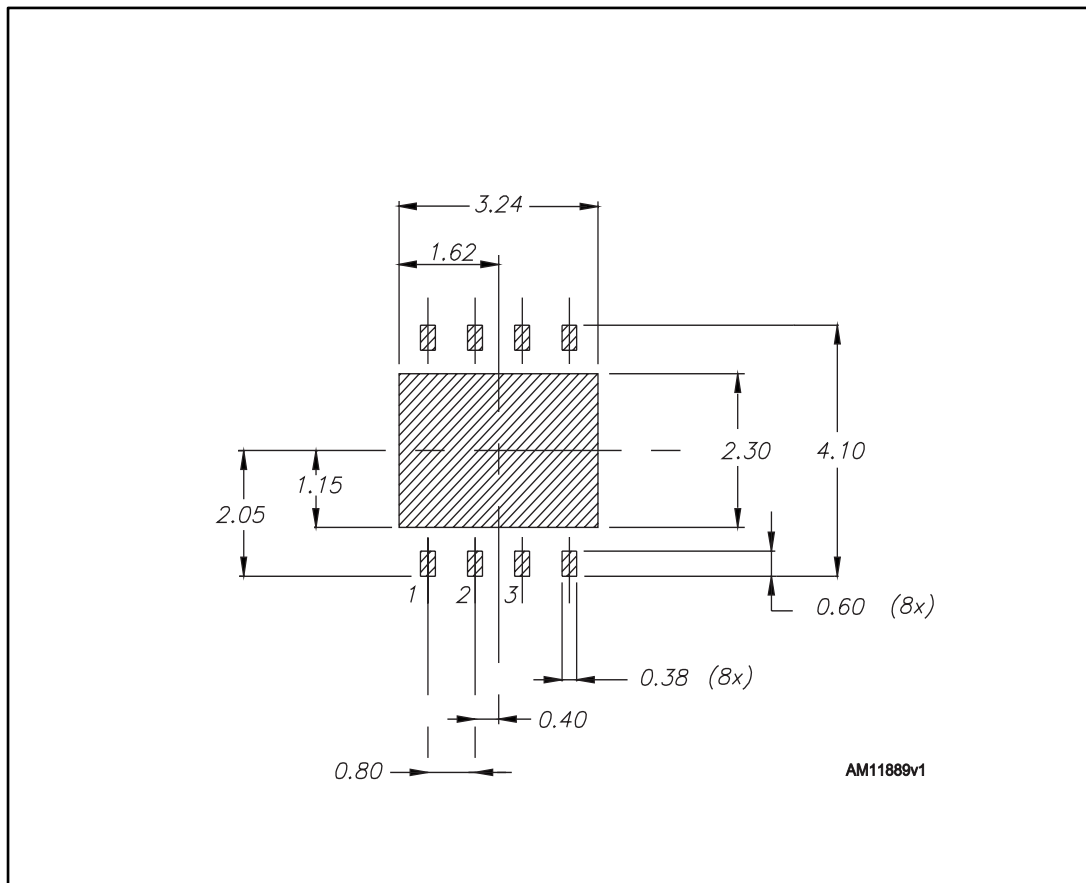


Table 8: DFN8 (4 x 4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0	0.02	0.05
A3		0,20	
b	0.23	0.30	0.38
D	3.90	4	4.10
D2	2.82	3	3.23
E	3.90	4	4.10
E2	2.05	2.20	2.30
e		0.80	
L	0.40	0.50	0.60

Figure 31: DFN8 (4 x 4 mm) footprint (all dimensions are in mm)



9 Packaging mechanical data

9.1 DFN6 (3 x 3 mm) tape and reel mechanical data

Figure 32: DFN6 (3 x 3 mm) tape

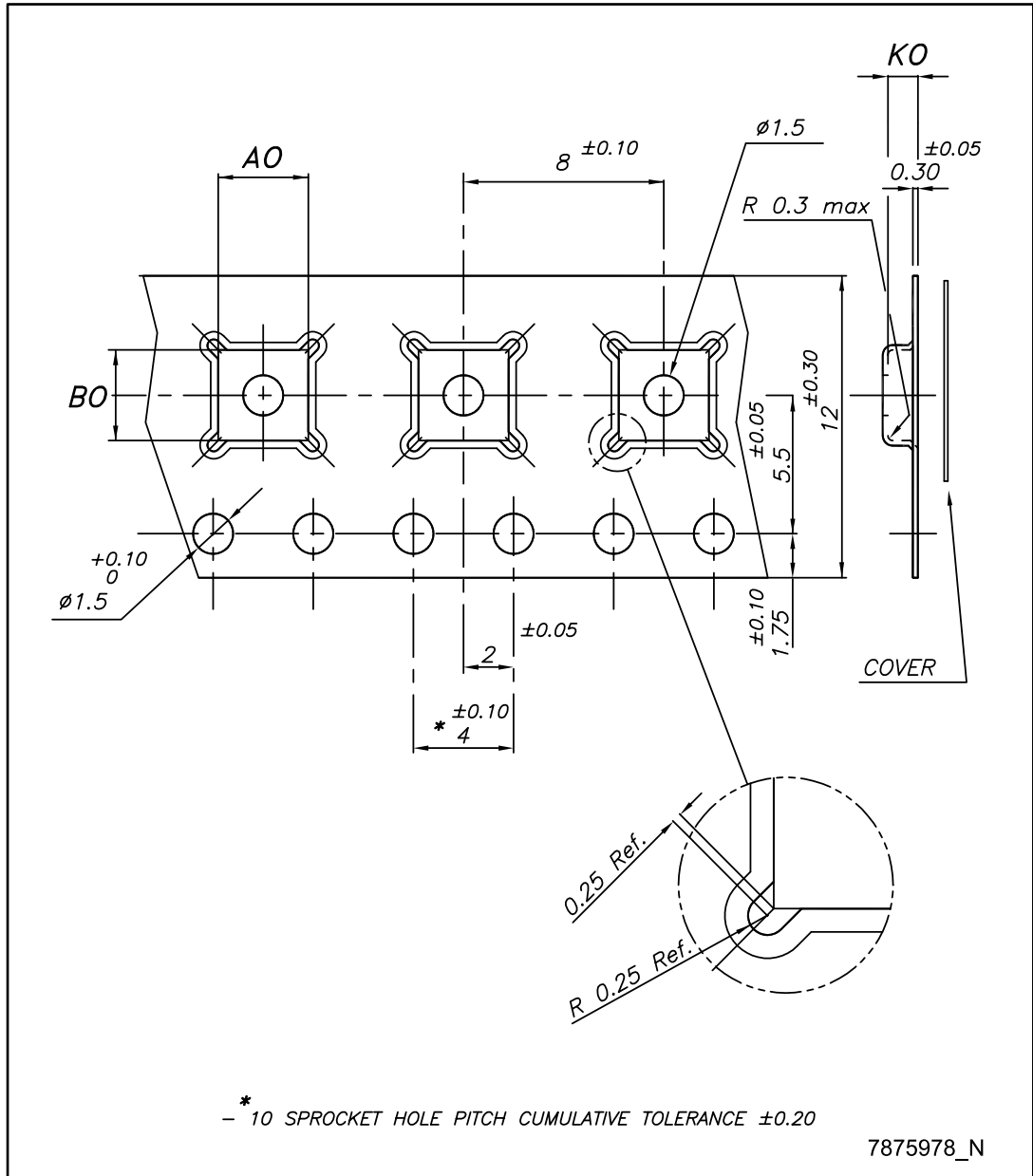


Figure 33: DFN6 (3 x 3 mm) reel

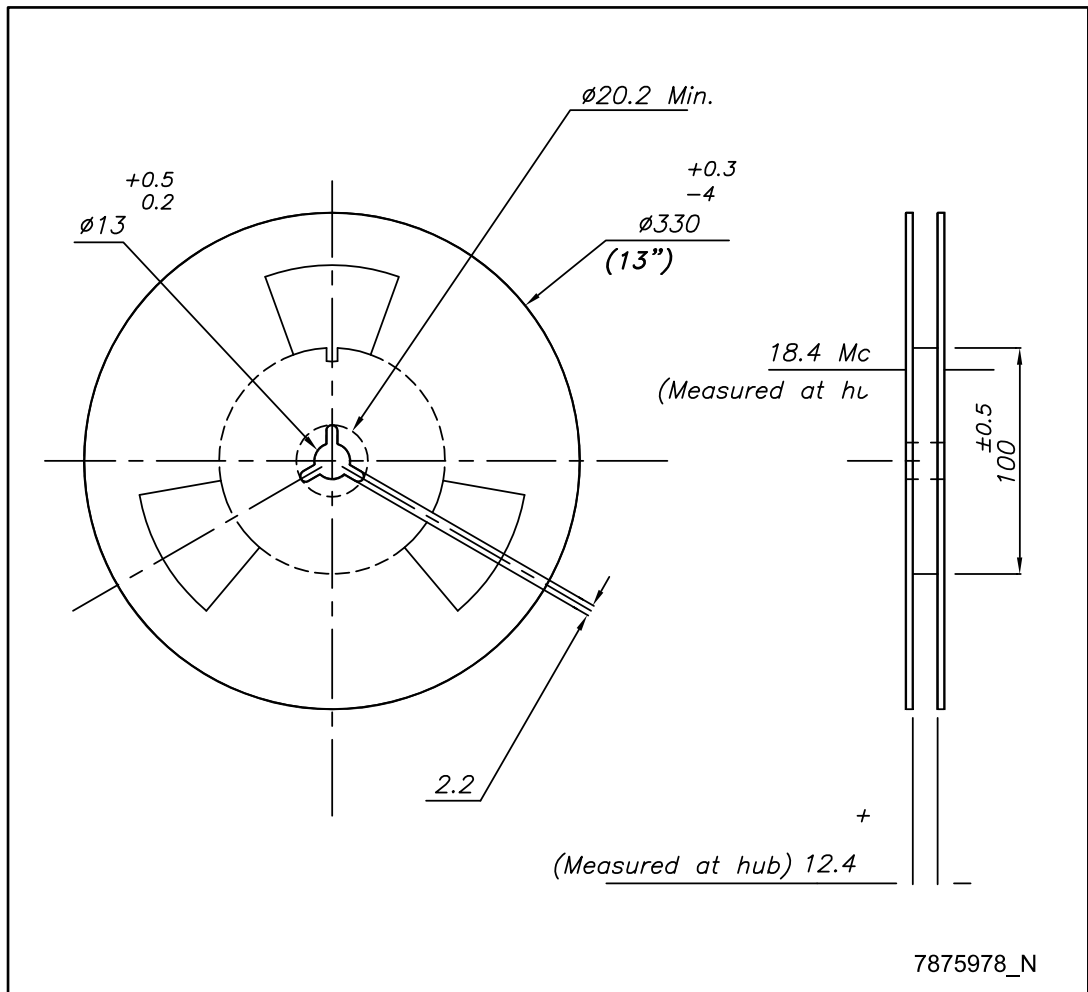


Table 9: DFN6 (3 x 3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

Figure 35: DFN8 (4 x 4 mm) reel

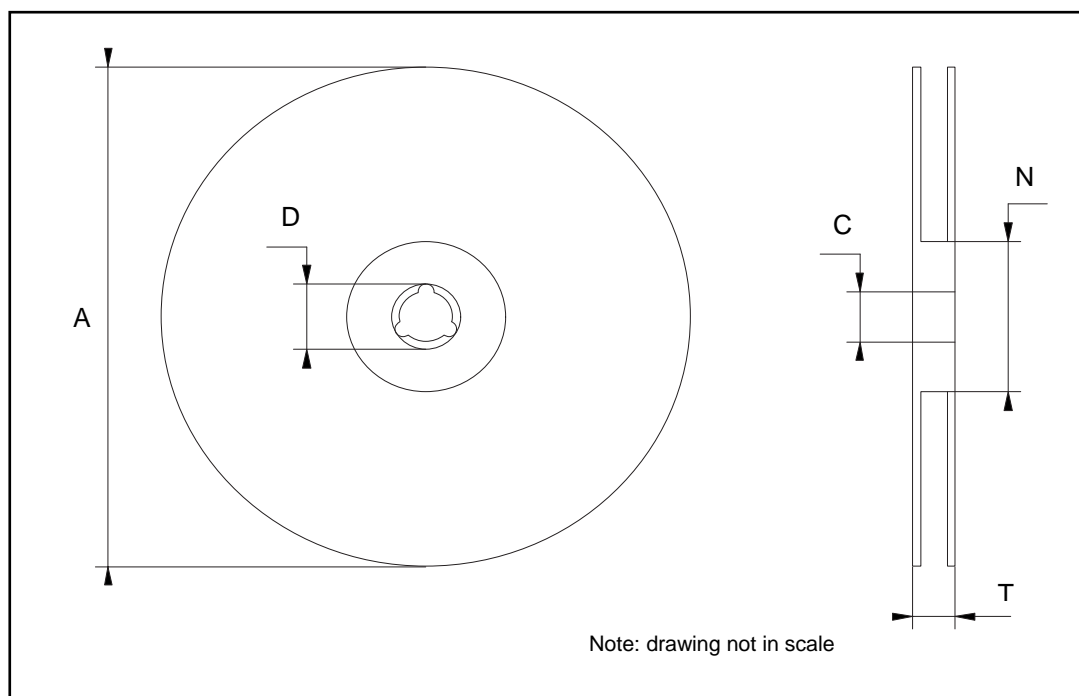


Table 10: DFN8 (4 x 4 mm) reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8	13.0	13.2
D	20.2		
N	60		
T			22.4

10 Ordering information

Table 11: Order codes

DFN6 (3 x 3 mm)	DFN8 (4 x 4 mm)	Output voltage
	LD39200DPUR	ADJ
LD39200PU33R		3.3 V

11 Revision history

Table 12: Document revision history

Date	Revision	Changes
28-Jul-2014	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved